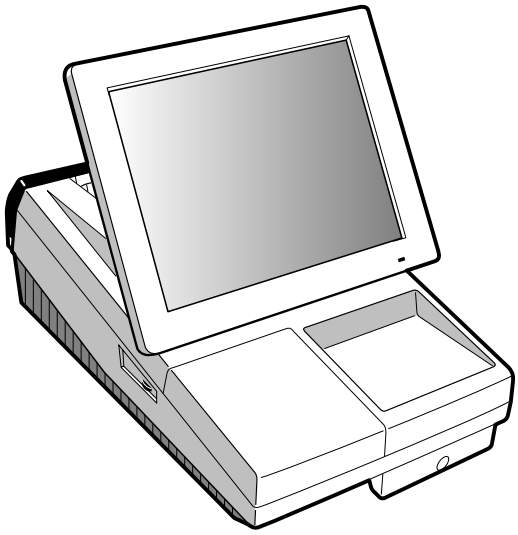
SHARP SERVICE MANUAL

CODE : 00ZUP5900VSME



POS TERMINAL

MODEL UP-5900

("V/VK" version)

CONTENTS

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PARTS GUIDE

Parts marked with "⚠" are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

This document has been published to be used for after sales service only.
The contents are subject to change without notice.

BATTERY DISPOSAL

Contains Nickel Metal Hydride Battery. Must be Disposed of Properly.
Contact Local Environmental Officials for Disposal Instructions.

CAUTION

RISK OF EXPLOSION IF BATTERY IS REPLACED
BY AN INCORRECT TYPE.
DISPOSE OF USED BATTERIES ACCORDING
TO THE INSTRUCTIONS.

AVOID: SHORT-CIRCUITING THE BATTERY TERMINALS.
KEEP THE BATTERY AWAY FROM FIRE.

∗ WHEN DISPOSING THE BATTERY, FOLLOW THE LOCAL
RULES AND REGULATIONS.

“BATTERY DISPOSAL”

THIS PRODUCT CONTAINS NICKEL-METAL HYDRIDE BATTERY.
THIS BATTERY MUST BE DISPOSED OF PROPERLY.
REMOVE THE BATTERY FROM THE PRODUCT AND CONTACT FEDERAL OR STATE ENVIRONMENTAL AGENCIES FOR INFORMATION ON RECYCLING AND DISPOSAL OPTIONS.

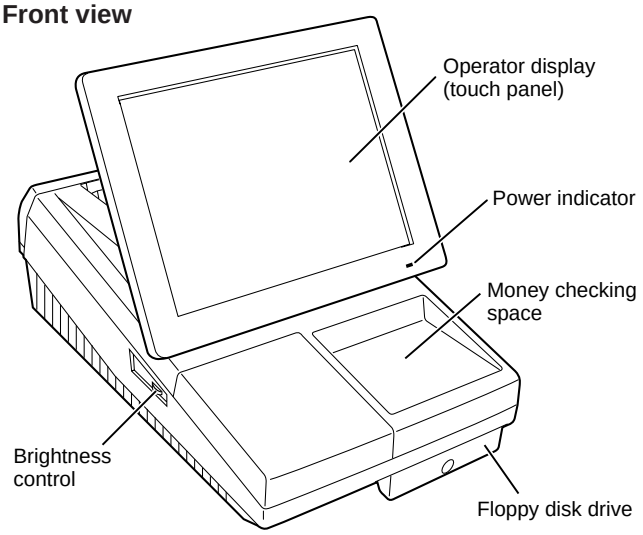
“TRAITEMENT DES ACCUMULATEUR USAGÉS”

CE PRODUIT CONTIENT UN ACCUMULATEUR À NICKEL MÉTAL HYDRIDE.
CET ACCUMULATEUR USAGÉ DOIT ÊTRE TRAITÉ CORRECTEMENT.
ENLEVEZ L’ ACCUMULATEUR DU PRODUIT ET PRENEZ CONTACT AVEC VOTRE AGENCE ENVIRONNEMENTALE LOCALE POUR DES INFORMATIONS SUR LES MÉTHODES DE RECYCLAGE ET DE TRAITEMENT.

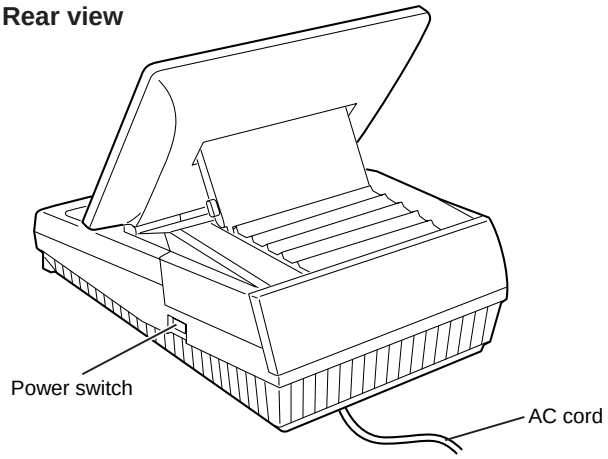
CHAPTER 1. SPECIFICATIONS

1. APPEARANCE

Front view



Rear view



AC cord

Plug your terminal into a wall outlet that has a dedicated ground before using.

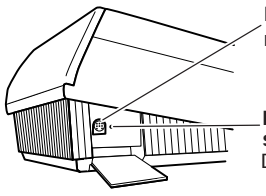
Power switch

Set the power switch to the ON (I) position after the terminal has been plugged in.

Power indicator

When the power switch is turned on, the power indicator will light up. The indicator will remain on even while the display's backlight is off.

Caution:



DO NOT insert any device into this connector unless recommended to do.
Doing so may cause the POS terminal not to function properly.

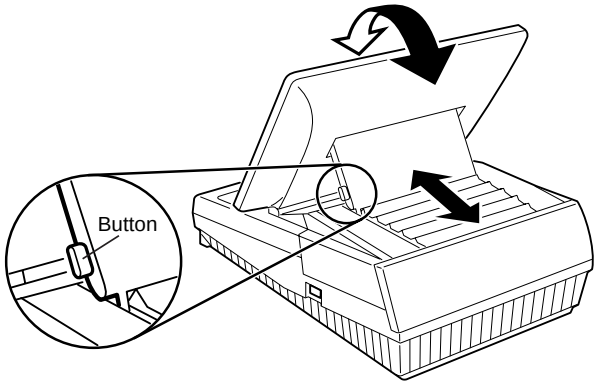
DO NOT insert any object into this switch unless instructed to do.
Doing so may damage or delete the data.

■ DISPLAY

Display angle

The display may be tilted for the best viewing angle by adjusting the rear stand.

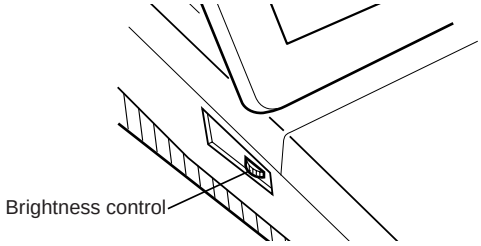
Be sure to push the release button on the side of the rear stand when sliding it.



Brightness control

The brightness of the illuminated display can be adjusted using the brightness control.

Turning the control backwards darkens the display and turning it forwards brightens the display.



Caution: The LCD module built in this POS terminal is manufactured with highly precise technology.
However bright pixels or blank pixels may appear. Also an irregular color and brightness may occur depending on the view angle. Please note that this type of phenomena is common for LCDs and may not be a malfunction.

The backlight in the display is a consumable part.

When the LCD display can no longer be adjusted and becomes darker, you should replace the LCD module. Consult your authorized SHARP dealer for further details.

2. RATING

ITEM	SPECIFICATIONS
External dimensions	11.8 (W) x 16.3 (D) x 13.5 (H) in. approximately (298.5 (W) x 415 (D) x 342 (H) mm)
Weight	Approximately 15.5lb. (7.0 kg)
Power source	220V~240V AC ± 10%, 50Hz/60Hz
Power consumption	Operating : 92.5W 590mA
Working temperature	32 to 104°F (0 to 40°C)

3. HARDWARE

3-1. DISPLAY

ITEM	SPECIFICATION	NOTE
Type	TFT color LCD with back light	High color (16bit) display
Screen size	12.1" full screen	
Dot size	0.0825 x RGB(W) x 0.2825(H) mm	
Resolution	XGA (1024 x 768 dots)	

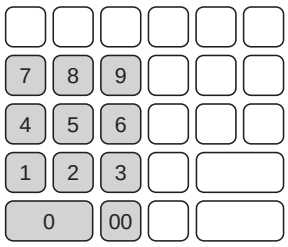
3-2. KEYBOARD

① TOUCH PANEL

ITEM	SPECIFICATIONS	NOTE
Type	Touch key (Analog touch panel)	
Number of key positions	4096 (W) x 4096 (H) positions	
Control	Mouse emulation	

② POS KEY PAD

VK (U. K.) version : Option (UP-C30PK)
Except VK version : Standard

ITEM	SPECIFICATION	NOTE
Type	POS rising keyboard	
Number of keys	Standard 27 keys	
	Numeric keys : 11 keys (1 to 9,0 and 00)	
	Capped keys : 16 keys (Key labels are locally purchased.)	
	Maximum 30 keys (6x5 matrix)	
	(Changing key layout by using ER-11KT7/12KT7/22KT7)	
Key layout		

3-3. PC SYSTEM

ITEM	SPECIFICATIONS	NOTE
CPU	Celeron processor	566MHz
Chip set	Intel 440BX + PIIX4e	
Graphic controller	SMI Lynx3DM4+	
Main memory (for executing MS-DOS, Application software)	Standard : 128 Mbytes	SD RAM
	Max. : 256 Mbytes	adding DIMM
Video RAM	4 Mbytes	Built-in type
BIOS ROM	512 Kbytes	Flash ROM
Keyboard controller	M38813	
Super I/O	PC87309	
POS system controller	PSC2 : LZ9AM22	

3-4. SERIAL PORT

D-SUB 9-pin connector COM1 and COM2 are equipped.

In order to supply +5V power, CI signal and +5V power supply of COM1 and COM2 can be switched.

2 channels of RJ45 Connector COM port are equipped.

COM3 or original I/O address (COM5) can be selected as the 1 channels of RJ45 COM port.

COM1 & COM2: D-sub 9 pin			
Pin No.	Signal	Function	I/O
1	CD	Data Carrier Detect	I
2	RD	Receive Data	I
3	SD	Send Data	O
4	ER	Data Terminal Ready	O
5	SG	Signal Ground	–
6	DR	Data set Ready	I
7	RS	Request to Send	O
8	CS	Clear to Send	I
9	CI/+5V	Ring Indicate / +5V	I/

COM3 (or COM5): Modular jack RJ45 8 pin			
Pin No.	Signal	Function	I/O
1	RS	Request to Send	O
2	ER	Data terminal Ready	I
3	SD	Send Data	O
4	SG/(+5V)	Signal Ground/(+5V)	–
5	SG	Signal Ground	–
6	RD	Receive Data	I
7	DR	Data set Ready	I
8	CS	Clear to Send	I

3-5. EXPANSION SLOT

5V PCI board can built in UP-5900 instead of an ISA PC board.

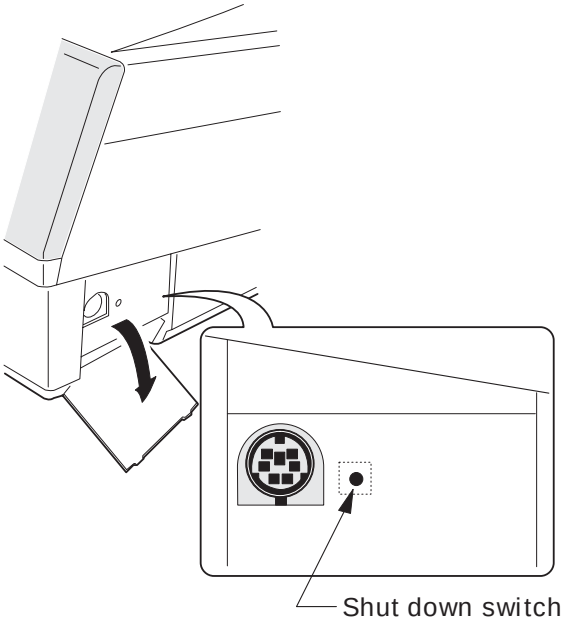
It has to satisfy with power consumption as follows.

ITEM	SPECIFICATION	NOTE
Type	PCI bus	
Power consumption	+5V max. 0.3A +12V max. 0.05A	
5V PCI board size	Short size PC board	(Local procurement item)
Quantity	1 slots	

3-6. SHUTDOWN SWITCH

The shutdown switch is used when the OS or application programs are straying and the system can not return to the normal state.

You must not use this shutdown switch when the UP-5900 is running normally. Use this switch only when the main power source is not cut off even if the main unit power switch is set to OFF position. The UP-5900 is turned OFF and the hardware is reset by turning the main power switch OFF and then pressing the shutdown switch.



[OUT LINE]

The shutdown switch is a single shut type. (Normally OFF position)

Push ON:	This position is used to reset the stand-by mode for power supply unit during software hang ups.
Release OFF:	Usually the shutdown switch needs to be set to this position when the UP-5900 is operating.

[OPERATING METHOD]

The shutdown switch is a push switch. If it is pushed to ON, the UP-5900 stops supplying the power when the power switch is set into stand-by mode.

Note: The shutdown operation will be ignored when the power switch is set to power-on position.

3-7. SYSTEM SWITCH

The system switches are used to preset various system configurations.

[OUT LINE]

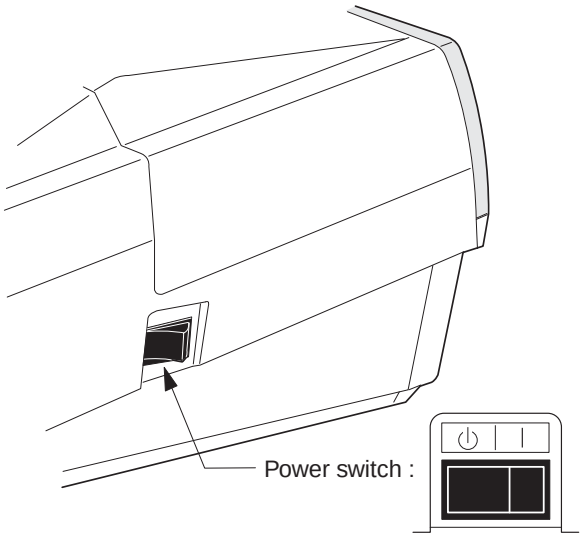
The system switches is short pin.

[JUMPER SWITCH]

JP1: Setting of IRQ allocated to COM3.
Position 1-2: COM3 = IRQ4
2-3: COM3 = IRQ11

JP2: Initialization of COMS.
Position 1-2: Initiallize
2-3: Not initiallize

3-8. POWER SWITCH



[OUT LINE]

The power switch has the positions ON and OFF (Stand-by)

ON position:	Usually the power switch needs to be set to this position when the POS-terminal is operated.
OFF position:	This position can be used to turn the stand-by mode. When the power switch is set to this position, the power supply stops automatically. But if the software program controls the power supply to hold, even if the power switch is set into this position, power supplying will be kept until a software program allows power supply to turn OFF.

[OPERATING METHOD]

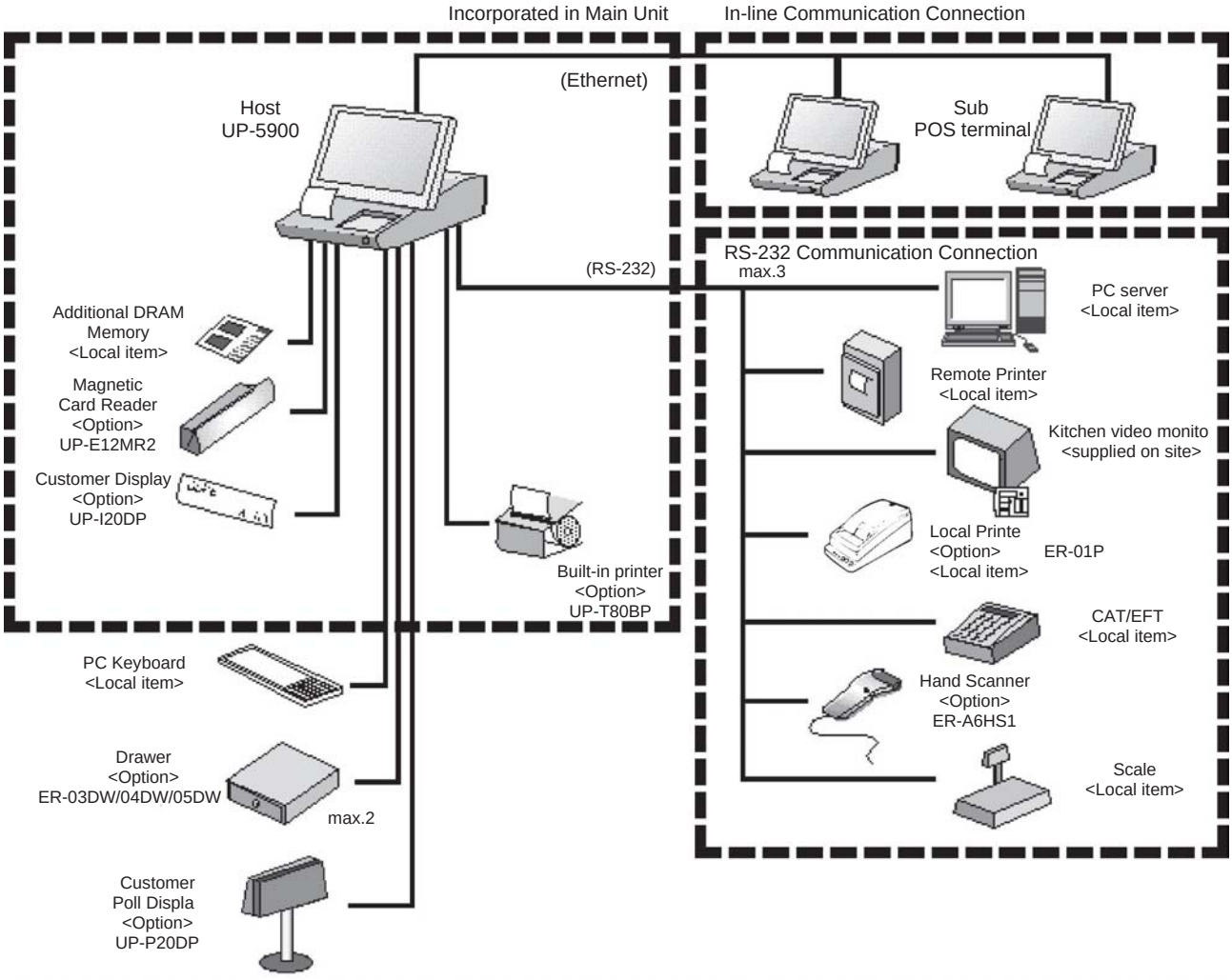
The power switch is a see-saw switch, and it can be tipped toward the ON or OFF.

4. SOFTWARE

ITEM		SPECIFICATION	NOTE
OS	provision	Windows 98 Second Edition	Local purchased (For V version) Provided from SHARP (For VK version)
	Available OS	Windows 2000	Local purchased
		Windows NT Work station 4.0	Local purchased
Device drivers	POS drivers	POS device driver	Provided from SHARP
		Touch panel driver	
		VGA device driver	
	Additional device driver		
BIOS			Written to the Flash ROM on the Main PWB.
Utility software		Touch panel calibration utility program	Provided from SHARP
		Double tap setup utility program	
		POS printer utility program	
Application software			Local purchased

CHAPTER 2. OPTIONS

1. SYSTEM CONFIGURATION



2. OPTIONS

No.	NAME	MODEL NAME	DESCRRIPTION
1	Customer display	UP-I20DP	2 line 20 digits dot display
2	Customer pole display	UP-P20DP	2 line 20 digits dot display
3	MCR (Magnetic Card Reader)	UP-E12MR2	for ISO 1 & 2 stripe card
4	Remote drawer	ER-03DW	4B/8C
		ER-04DW	4B/8C
		ER-05DW	5B/8C
5	Receipt/Journal printer	ER-01PU	2 station (R/J) thermal printer 45mm width
6	Built-in printer	UP-T80BP	1 station thermal printer 80mm width
7	Hand scanner	ER-A6HS1	for reading bar code
8	Key pad (Option for VK version)	UP-C30PK	Std. 27 keys, Max. 30 keys
9	Key kit (Used for key pad : UP-C30PK)	ER-11KT7	1 x 1 key top kit
		ER-12KT7	1 x 2 key top kit
		ER-22KT7	2 x 2 key top kit

3. LOCALLY SUPPLIED OPTIONS

No.	NAME	DESCRIPTION	NOTE
1	DIMM	168pin SD-RAM	Max. 256Mbytes *1
2	Hard disk drive	2.5 inch type	*2
3	PC keyboard	PS/2 type PC keyboard	
4	Application software		
5	Additional device drivers		

***1 Extension RAM module**

[Device] 168pin DIMM

[Outline] UP-5900 has a socket as DIMM.
The following DIMM memory specification must be adhered to.

[Specification]

	168pin.DIMM
Type	SD-RAM type
Access time	PC100 (more than)
Power	3.3V
Refresh cycle	4096/64 msec.
Refresh type	AUTO
Power consumption	1400 mA (less than)

***2 Hard disk drive**

[Device] 2.5 inch type Hard disk drive

[Outline] It is necessary to satisfy with 2.5 inch Hard disk drive specification as follows.

[Specification]

	2.5 inch Hard disk drive
Maker	Fujitsu
Model	MHN2150AT
Capacity	15 Gbytes
Interface	ATA-4

4. SERVICE OPTIONS

No	NAME	PARTS CODE	PRICE	DESCRIPTION
1	Connector cable for Dongle (LPT-1)	QCNW-7858BHZZ	BL	Relay line from Terminal to Dongle
2	1 hole clerk key The key No.1 to No.12 are supplied together with UP-5900.	LKGiM1004BH13	BH	Key No.13
		LKGiM1004BH14	BH	Key No.14
		LKGiM1004BH15	BH	Key No.15
		LKGiM1004BH16	BH	Key No.16
		LKGiM1004BH17	BH	Key No.17
		LKGiM1004BH18	BH	Key No.18
		LKGiM1004BH19	BH	Key No.19
		LKGiM1004BH20	BH	Key No.20
		LKGiM1004BH21	BH	Key No.21
		LKGiM1004BH22	BH	Key No.22
		LKGiM1004BH23	BH	Key No.23
		LKGiM1004BH24	BH	Key No.24
		LKGiM1004BH25	BH	Key No.25
		LKGiM1004BH26	BH	Key No.26
		LKGiM1004BH27	BH	Key No.27
		LKGiM1004BH28	BH	Key No.28
		LKGiM1004BH29	BH	Key No.29
		LKGiM1004BH30	BH	Key No.30
		LKGiM1004BH31	BH	Key No.31
		LKGiM1004BH32	BH	Key No.32
		LKGiM1004BH33	BH	Key No.33
		LKGiM1004BH34	BH	Key No.34
		LKGiM1004BH35	BH	Key No.35
		LKGiM1004BH36	BH	Key No.36
		LKGiM1004BH37	BH	Key No.37
		LKGiM1004BH38	BH	Key No.38
		LKGiM1004BH39	BH	Key No.39
		LKGiM1004BH40	BH	Key No.40
		LKGiM1004BH41	BH	Key No.41
		LKGiM1004BH42	BH	Key No.42
		LKGiM1004BH43	BH	Key No.43
		LKGiM1004BH44	BH	Key No.44
		LKGiM1004BH45	BH	Key No.45
		LKGiM1004BH46	BH	Key No.46
		LKGiM1004BH47	BH	Key No.47
		LKGiM1004BH48	BH	Key No.48
		LKGiM1004BH49	BH	Key No.49

No	NAME	PARTS CODE	PRICE	DESCRIPTION
		LKGiM1004BH50	BH	Key No.50
		LKGiM1004BH51	BH	Key No.51
		LKGiM1004BH52	BH	Key No.52
		LKGiM1004BH53	BH	Key No.53
		LKGiM1004BH54	BH	Key No.54
		LKGiM1004BH55	BH	Key No.55
		LKGiM1004BH56	BH	Key No.56
		LKGiM1004BH57	BH	Key No.57
		LKGiM1004BH58	BH	Key No.58
		LKGiM1004BH59	BH	Key No.59
		LKGiM1004BH60	BH	Key No.60
		LKGiM1004BH61	BH	Key No.61
		LKGiM1004BH62	BH	Key No.62
		LKGiM1004BH63	BH	Key No.63
		LKGiM1004BH64	BH	Key No.64
		LKGiM1004BH65	BH	Key No.65
		LKGiM1004BH66	BH	Key No.66
		LKGiM1004BH67	BH	Key No.67
		LKGiM1004BH68	BH	Key No.68
		LKGiM1004BH69	BH	Key No.69
		LKGiM1004BH70	BH	Key No.70
		LKGiM1004BH71	BH	Key No.71
		LKGiM1004BH72	BH	Key No.72
		LKGiM1004BH73	BH	Key No.73
		LKGiM1004BH74	BH	Key No.74
		LKGiM1004BH75	BH	Key No.75
		LKGiM1004BH76	BH	Key No.76
		LKGiM1004BH77	BH	Key No.77
		LKGiM1004BH78	BH	Key No.78
		LKGiM1004BH79	BH	Key No.79
		LKGiM1004BH80	BH	Key No.80
		LKGiM1004BH81	BH	Key No.81
		LKGiM1004BH82	BH	Key No.82
		LKGiM1004BH83	BH	Key No.83
		LKGiM1004BH84	BH	Key No.84
		LKGiM1004BH85	BH	Key No.85
		LKGiM1004BH86	BH	Key No.86
		LKGiM1004BH87	BH	Key No.87
		LKGiM1004BH88	BH	Key No.88
		LKGiM1004BH89	BH	Key No.89
		LKGiM1004BH90	BH	Key No.90
		LKGiM1004BH91	BH	Key No.91
		LKGiM1004BH92	BH	Key No.92
		LKGiM1004BH93	BH	Key No.93
		LKGiM1004BH94	BH	Key No.94
		LKGiM1004BH95	BH	Key No.95
		LKGiM1004BH96	BH	Key No.96
		LKGiM1004BH97	BH	Key No.97
		LKGiM1004BH98	BH	Key No.98
		LKGiM1004BH99	BH	Key No.99

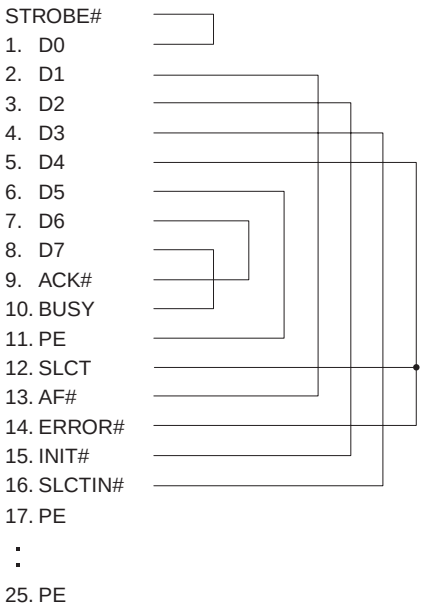
No	NAME	PARTS CODE	PRICE	DESCRIPTION
		LKGiM1004BH00	BH	Key No.100
		LKGiM1004BHA1	BH	Key No.101
		LKGiM1004BHA2	BH	Key No.102
		LKGiM1004BHA3	BH	Key No.103
		LKGiM1004BHA4	BH	Key No.104
		LKGiM1004BHA5	BH	Key No.105
		LKGiM1004BHA6	BH	Key No.106
		LKGiM1004BHA7	BH	Key No.107
		LKGiM1004BHA8	BH	Key No.108
		LKGiM1004BHA9	BH	Key No.109
		LKGiM1004BHA0	BH	Key No.110
		LKGiM1004BHB1	BH	Key No.111
		LKGiM1004BHB2	BH	Key No.112
		LKGiM1004BHB3	BH	Key No.113
		LKGiM1004BHB4	BH	Key No.114
		LKGiM1004BHB5	BH	Key No.115
		LKGiM1004BHB6	BH	Key No.116
		LKGiM1004BHB7	BH	Key No.117
		LKGiM1004BHB8	BH	Key No.118
		LKGiM1004BHB9	BH	Key No.119
		LKGiM1004BHB0	BH	Key No.120
		LKGiM1004BHC1	BH	Key No.121
		LKGiM1004BHC2	BH	Key No.122
		LKGiM1004BHC3	BH	Key No.123
		LKGiM1004BHC4	BH	Key No.124
		LKGiM1004BHC5	BH	Key No.125
		LKGiM1004BHC6	BH	Key No.126

5. SERVICE TOOLS

No.	NAME	PARTS CODE	PRICE	DESCRIPTION
1	Parallel loop back connector	UKOG-2366BHZZ	BM	
2	MCR test card	UKOG-6718RCZZ	BE	for UP-E12MR2
3	RS232 loop back connector	UKOG-6705RCZZ	BC	for RS232 connector
4	RS232 modular jack loop back connector	UKOG-6729BHZZ	AZ	for RJ45 connector
5	TOUCH PEN	CPENP1004PCN5	AG	

5-1. PARALLEL LOOP BACK CONNECTOR: UKOG-2366BHZZ

This connector is connected between CN10/11 of the main PWB and the parallel port through the Dongle cable (QCNW-7858BHZZ) for checking the parallel port during execution of diagnostics.



5-2. MCR TEST CARD: UKOG-6718RCZZ

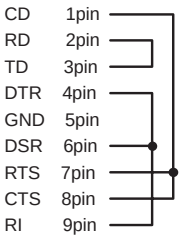
- Used when executing the diagnostics of the UP-E12MR2.
- External view



5-3. RS232 LOOP BACK CONNECTOR: UKOG-6705RCZZ

Connected to the RS232 connector (D-SUB 9 pin: COM1, COM2) of the UP-5900 and ER-A8RS, and used to check loop signals when executing diagnostics.

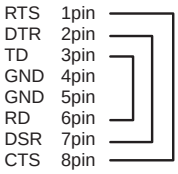
- Connection diagram



5-4. RS232 MODULAR JACK LOOP BACK CONNECTOR: UKOG-6729BHZZ

Connected to the RS232 connector (RJ45: COM3) of the UP-5900, and used to check loop signals when executing diagnostics.

- Connection diagram



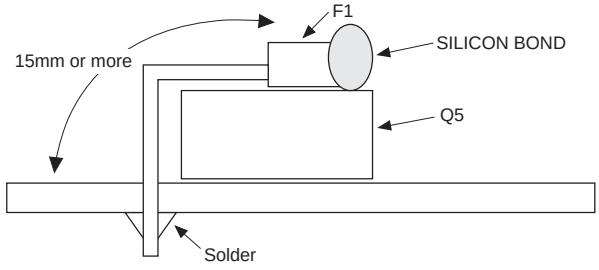
CHAPTER 3. SERVICE PRECAUTION

1. CONDITIONS FOR SOLDERING CIRCUIT PARTS

To solder the following parts manually, follow the conditions described below.

PARTS NAME	PARTS CODE	LOCATION	CONDITIONS FOR SOLDERING
Ceramic oscillator	RCRMZ7002RCZZ	TOUCH PANEL CONTROL PWB: X1 (8M)	270°C/3sec.
	RCRMZ7004RCZZ	MAIN PWB: X4 (8M)	
	RCRMZ7004RCZZ	MAIN PWB: X3 (7.37M)	
Thermal fuse	QFS−T0096FCZZ	MAIN PWB: F1	300°C/3sec (Length of lead: 15mm or more)

Thermal fuse installation fig



2. CAUTIONS ON HANDLING CPU AND POWER FAN

- When removing or performing maintenance activities on the CPU and POWER FAN, be sure to handle them with care, because it may cause abnormal sounds or deteriorate their performance if they are dropped or exposed to a heavy impact.

3. NOTE FOR HANDLING OF TOUCH PANEL

- The transparency of the touch panel should be vitally important. Use clean gloves and masks.
- For handling, do not hold the transparent area, and do not hold the heat seal connector section to assure reliability.
- Do not overlay touch panels. The edge may damage the surface.
- Do not place heavy things on the touch panel.
- Do not apply a strong shock, and do not drop it.
- When attaching the protection film again, carefully check for dirt. If there is any dirt, it is transferred.
- To clean dirt on the surface, use a dry, soft cloth or a cloth immersed in ethyl alcohol.
- Check that the housing does not give stress to the touch panel.
- Be careful not to touch the touch panel with tools.
- The heat seal section is easily disconnected. Be careful not to place stress to the heat seal section when installing.
- The touch panel is provided with an air groove to make the external and the internal air pressure equal to each other. If water or oil is put around the air groove, it may penetrate inside. Be careful to keep the air groove away from water and oil.
- Do not use sharp objects when making input entrees.

4. NOTE FOR HANDLING OF LCD

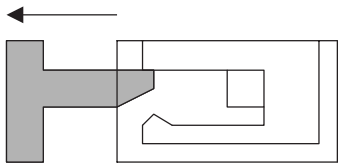
- The LCD elements are made of glass. BE careful not to expose them to strong mechanical shock, or they may be broken. Use extreme care not to break them.
- If the LCD element is broken and the liquid leaks, avoid contact with your mouth or eyes. If the liquid comes in contact with your skin or clothes, immediately clean with soap.
- Use the unit under the rated conditions to prevent against damage.
- Be careful not to place water or other liquids on the display surface.
- The reflection plate and the polarizing plate are easily scratched. BE careful not to touch them with a hard object such as glass, tweezers etc. Never hit, push, or rub the surface with hard objects.
- When installing the unit, be careful not to apply stress to the LCD module. If excessive stress is applied, abnormal display or uneven color may result.

5. CAUTIONS ON HANDLING FFC

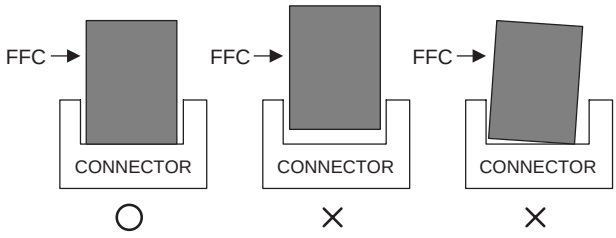
When connecting or disconnecting the ffc, follow the procedures below.

∗ How to insert FFC

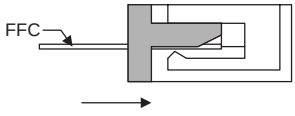
(1) Pull the slider to the unlock position.



(2) Inserting the FFC
Insert the FFC firmly until the FFC hits the bottom of the connector's insulator.



(3) Close the slider to the lock position



6. PS2 KEYBOARD USABLE FOR UP-5900

The UP-5900 can be externally connected to a keyboard.

The UP-5900's key BIOS conforms to the PC standard, but this BIOS's operation is not compatible for some keyboards.

Some keyboards may cause operation errors due to delicate timing and conflicts.

It is currently found that the following models of keyboards may malfunction.

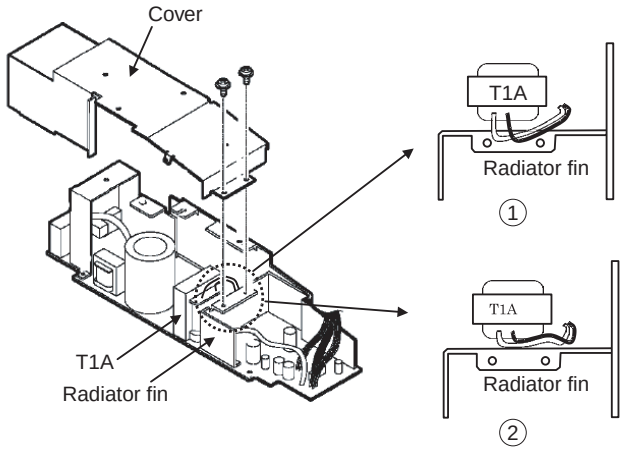
When selecting a keyboard to be connected, test the keyboard in advance to check that it correctly works.

- Japanese keyboard (106 keys)
  Manufactured by IBM: TYPE/MODEL5576-B01 FRUPN66G0507
- English keyboard (101 keys)
  Manufactured by NMB Technologies Inc.: Model: RT6651T+

7. PRECAUTION FOR ATTACHING THE COVER TO THE POWER UNIT

When attaching the cover to the power unit, two lead wires (white x 1, black x 1) of T1A (transformer) in the power unit may be pinched by the cover, causing a damage to the wiring. (①)

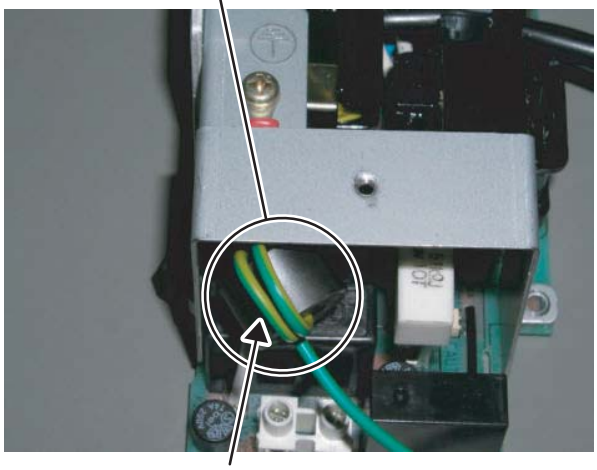
To avoid this, push two lead wires of T1A between the radiator fin and T1A before attaching the cover. (②)



8. AC CORD GND WIRE CORE ADDITION

Add the core to the AC cord GND wire for increasing the EMI margin.

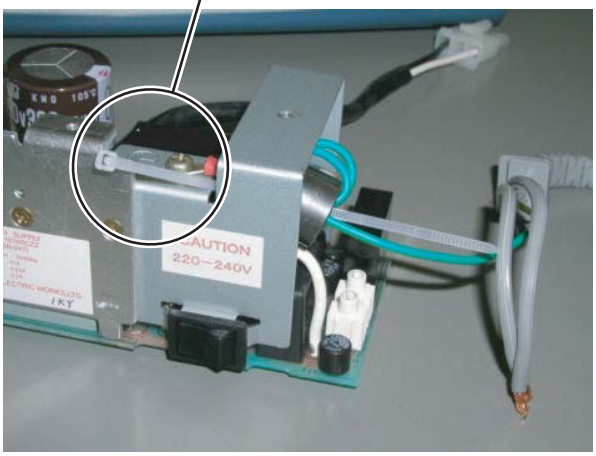
Core added: SC18B (RCORF6698BHZZ)



Wind the AC GND wire around the core 3 turns (2 windings).

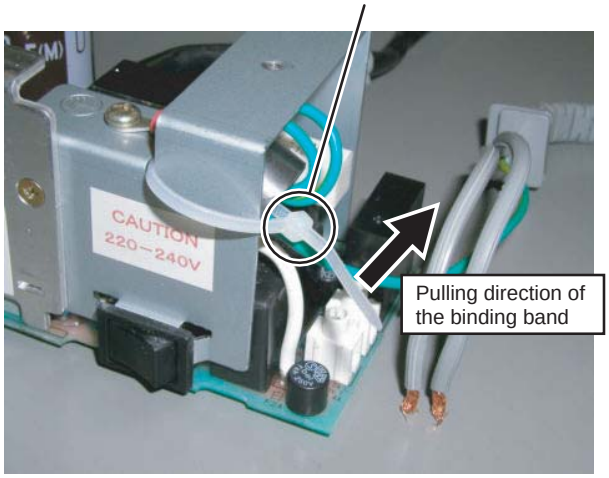
■Fixing the core

Binding band



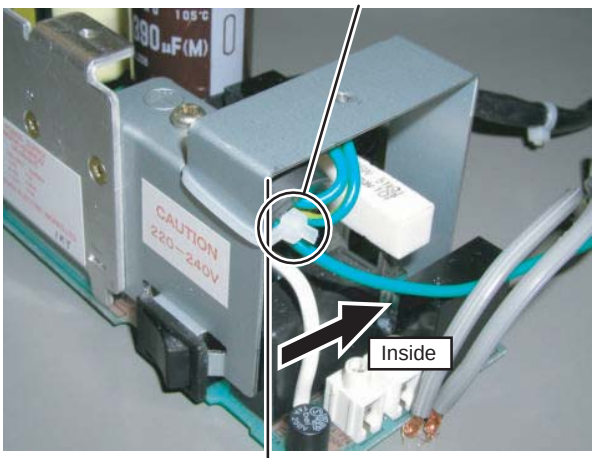
Procedure ①

Binding position of the binding band



Procedure ②

Binding position of the binding band



The binding position of the band must be inside of this position.

Procedure ③

Procedure ① Pass the binding band through the core as shown in the photo.

Procedure ② Bind the core as shown in the photo and pull the band to fix.

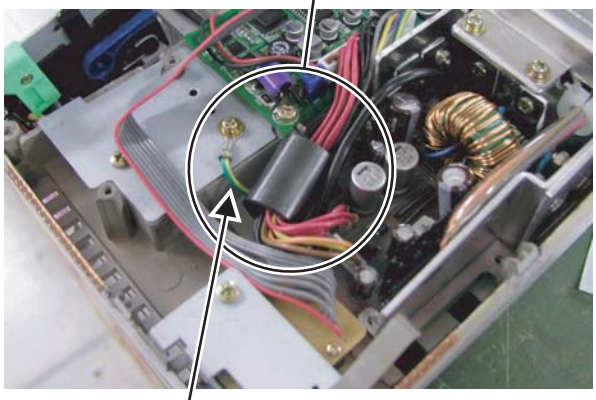
Procedure ③ Fix so that the binding position of the band does not extend out of the plate.

■Power unit - Main PWB unit connection cable core change

1. Content of change

   The core of the cable connecting the power unit and the main PWB unit is changed.

Core: RCORF2356BHZZ(SC18E)
Pass all the cables (1pin - 15pin) through the core (SC18E) except for the power cable. At that time, be careful not to apply an external force to the power unit capacitor.



This cable is passed under the PS unit - Main PWB cable.

■LCD cable treatment

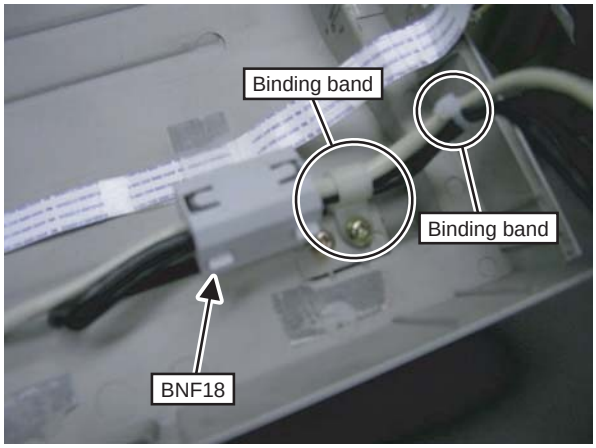


Fig.1 LCD cable treatment and core addition

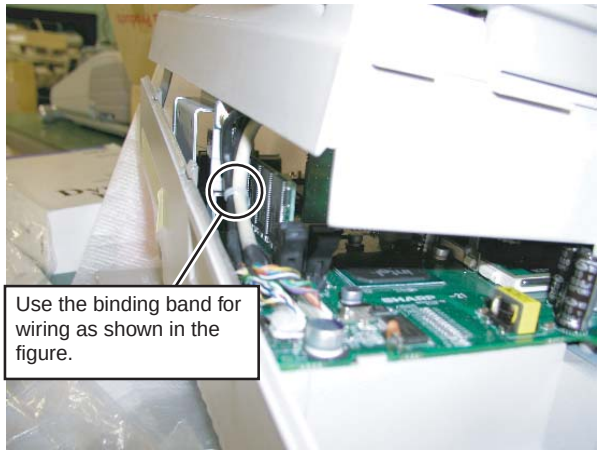


Fig.2 LCD cable treatment (Cable and riser fixing)

30PK standard destination model

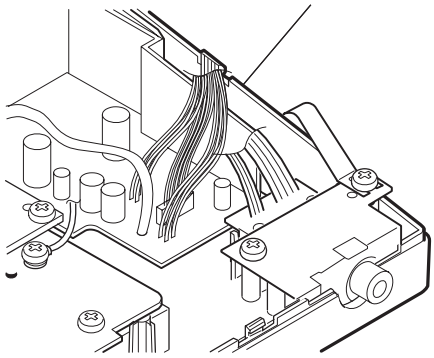


Fig.4 Earth Spring 1 (30PK)

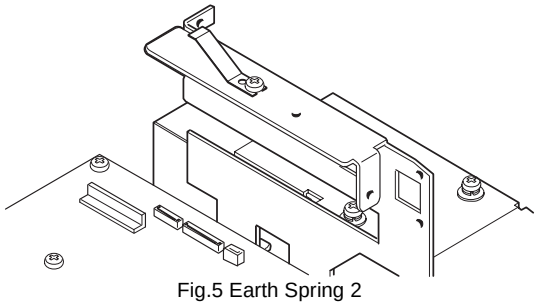


Fig.5 Earth Spring 2

∗Earth Spring 1 and 2 are the same one.

∗Earth Spring 1 in Fig.4 is packed together with 30PK.

CHAPTER 4. DIAGNOSTICS SPECIFICATIONS

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■ DIAGNOSTICS PROGRAM: CREATING AN MS-DOS STARTING MEDIA (FD)

Before executing the Diagnostic program, you must create the MS-DOS starting media and copy the Diagnostics program onto it.

HOW TO CREATE AN MS-DOS STARTING MEDIA

1) Execute the command given below on the PC where the MS-DOS Ver. 6.22 is running and create an MS-DOS starting media (FD).

   MS-DOS (Command) format a: /s

2) Copy the Diagnostics program onto the MS-DOS starting media (FD).

1. GENERAL

This diagnostic program is used to check the PWB's, the process, and the machine of the UP-5900 series in a simplified manner.

This test program is supplied with floppy disks.

2. SYSTEM CONFIGURATION

The system requires the POS terminal, and a PS2 keyboard for diagnostic operations.

3. SERVICE DIAGNOSTICS

3-1. SERVICE DIAGNOSTICS GETTING STARTED

GETTING STARTED:

Execute “SRV.BAT” by entering the command with the PS2 keyboard as follows:

A:\> SRV ↵

“A:\>” is the DOS prompt. (Used by the FD)

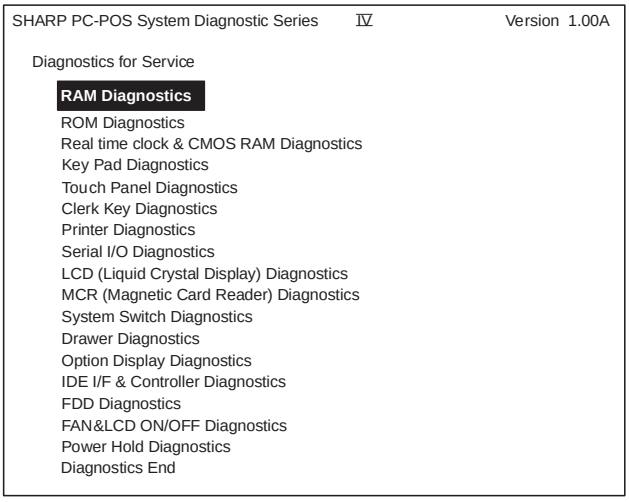
∗Do not load any device drivers when using this program.

∗To operate other applications after performing this program, it is recommended to re-boot the machine.

3-2. SELECTION MENU

The diagnostics menu is started and the following menu is displayed.

The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the PS2 keyboard. Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program. When the selected diagnostics program is completed, the display returns to the menu screen by pressing the ESC key. Select “Diagnostics End” and press the Enter key to terminate the diagnostics.



3-3. RAM DIAGNOSTICS

This program is used to test the standard memory and the extension memory.

1) D-RAM CHECK

① Checking content

All memory areas are checked in blocks of 512KB. The checking procedures are as follows:

i. Test data 5555H is written to all the test areas.

ii. Test data and read data are compared by each word, If it is O.K., test data AAAAH is written to the test area.

iii. Test data and read data are compared by each word, If it is O.K., test data 5555H is written to the test area.

iv. Test data 0000H is written to all the test areas.

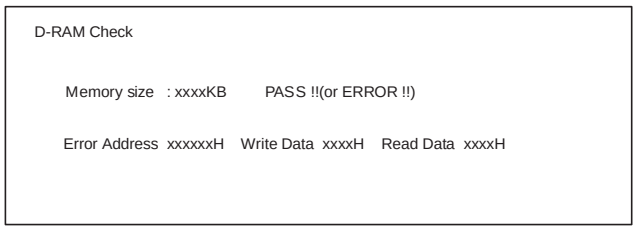
v. Test data and read data are compared by each word, If it is O.K., test data FFFFH is written to the test area.

vi. Test data and read data are compared by each word, If it is O.K., test data 0000H is written to the test area.

When an error occurs during the test, the error address and data are displayed and the test is stopped.

For the extended memory test, the value is set in the setup of the read test and is made to the area in increments of 512KB.

② Display



The error address and the error data are displayed only when an error occurs. (When no errors occur, they are not displayed.)

③ Terminating method

After completion of the test, press the Esc key to terminate and return to the service diagnostics menu.

3-4. ROM DIAGNOSTICS

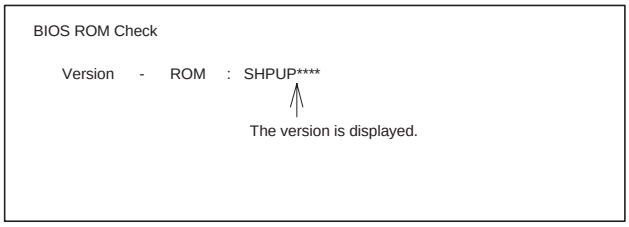
The BIOS ROM, is tested.

1) BIOS ROM CHECK

① Checking content

The BIOS ROM version is displayed.

② Display



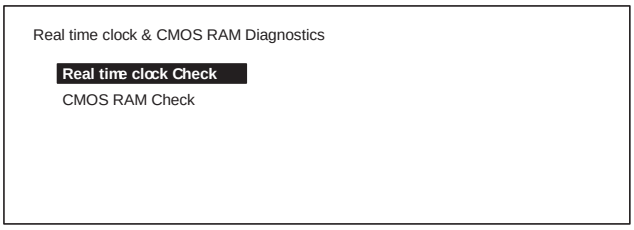
③ Terminating method

After the test result is displayed, press Esc key to terminate and return to the service diagnostics menu.

3-5. REAL TIME CLOCK & CMOS RAM DIAGNOSTICS

RTC and CMOS RAM check is performed.

The following menu is displayed. The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the PS2 keyboard. Move the cursor to the desired item, and then press the Enter key to execute the selected diagnostics program. When the selected diagnostics program is completed. Pressing the Esc key again returns to the service diagnostics menu.

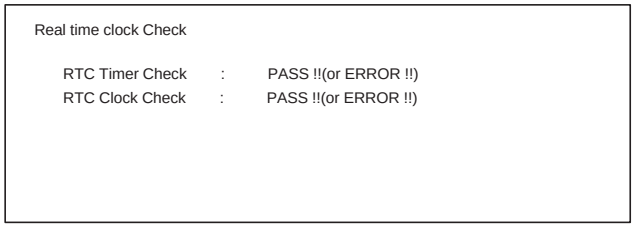


1) REAL TIME CLOCK CHECK

① Checking content

RTC timer function and RTC clock function are tested.

② Display



③ Terminating method

After the test result is displayed, press the Esc key to terminate and return to the RTC and CMOS RAM diagnostics menu.

2) CMOS RAM CHECK

① Checking content

The read/write check is performed for the CMOS-RAM when setting up. The checking procedure is as follows:

i. Test address data is saved to the main memory.

ii. Test data 55H is written to the test address.

iii. Test data and read data are compared, and test data AAH is written to the test address.

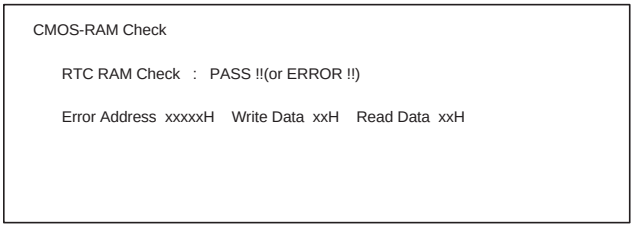
iv. Test data and read data are compared.

v. The saved test data is written to the test area.

vi. The address is incremented until it becomes 3FH.

If POFF interruption is generated during the test, the test is stopped and the saved data is written to the test area within 50ms.

② Display



The error address and error bit are displayed only when an error occurs. (When no error occurs, they are not displayed.)

③ Terminating method

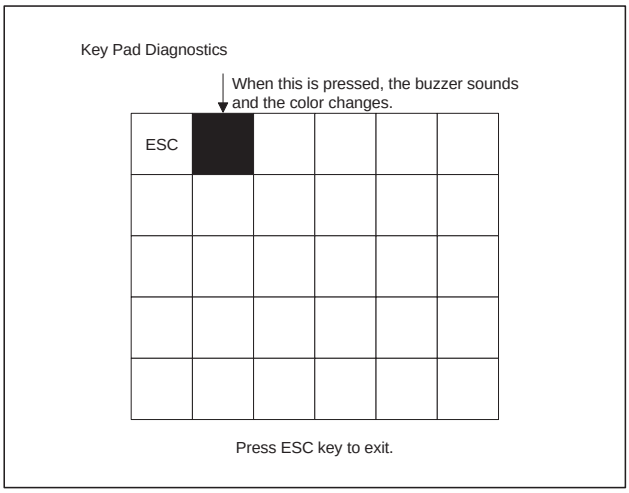
After the test result is displayed, press the Esc key to terminate and return to the RTC and CMOS RAM diagnostics menu.

3-6. KEY PAD DIAGNOSTICS

1) KEY PAD CHECK

The UP-C30PK key test is performed. In the UP-C30PK, keys are detected by matrix scan of KBC (M38802M270).

① Display



② Content

When a key is pressed, its color changes and the key catch sound is made.

The keys to be checked and their positions are as shown below.

ESC	F4	F5	F10	Delete	Back Space
7	8	9	Tab	↑	↓
4	5	6	L-Shift	←	→
1	2	3	L-Ctrl	Space	
0		•	L-Alt	Enter	

③ End

Press the ESC key to terminate the test.

3-7. TOUCH PANEL DIAGNOSTICS

The touch panel and its controller are checked. Communication with the controller is performed by the 8250 built in the gate array PSC2.

The controller diag check, the touch keypad test, and the linearity test are performed.

The initial display is as follows:



1) CONTROLLER DIAGNOSTICS TEST

① Checking content

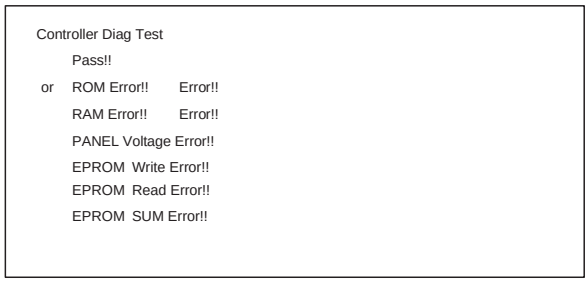
After initializing the controller, the diagnostic command is executed. The procedures are as follows:

- One byte of sample data (FFh) is sent and a wait state of 100ms is made.
- The reset command (80h) is sent and a wait state for the end code (2 bytes: 90h and 00h) from the controller is made.
- The diagnostic command (2 bytes: 89h, any one-byte data) is executed, and a wait state for the end code (3 bytes: 90h, return code, any one-byte data) is made.
- If an error occurs the error display is made with the return code.

∗ To exit from the controller diagnostic test, press the Esc key during the wait state for the end code response.

Return code	Content
0Ah	ROM error
0Bh	RAM error
0Ch	Panel voltage error
0Dh	Reserve
0Eh	EPROM write error
0Fh	EPROM read error
10h	EPROM check sum error

② Display



③ Terminating method

After the test result is displayed, press the Esc key to terminate and return to the Touch panel diagnostics menu.

2) TOUCH KEY PAD TEST

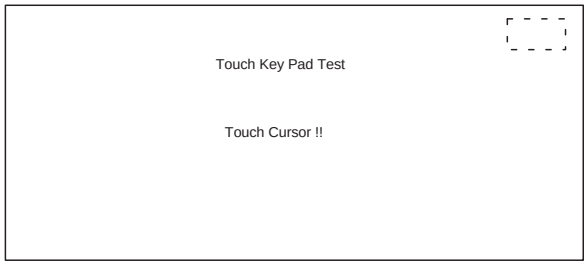
① Checking content

The driver function call is used. The [ ] is displayed at the four corners of the LCD sequentially.

(In the sequence of upper right, upper left, lower left, lower right.)

When the [ ] is touched by the operator, the buzzer sounds and the screen turns to ■ .

② Display



③ Terminating method

Touch all four [ ] areas or press the Esc key to terminate and return to the Touch panel diagnostics menu.

3) LINEARITY TEST

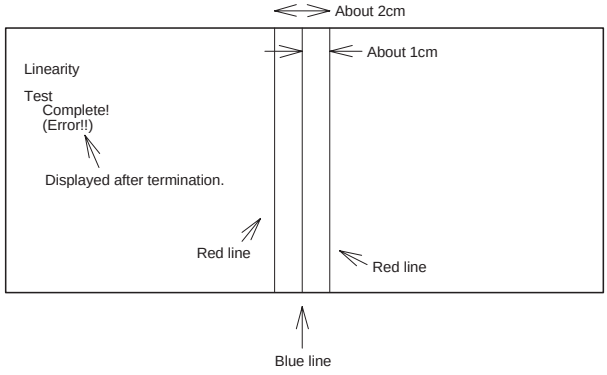
① Checking content

Red lines are displayed at both sides of the blue line at the center. The operator must touch the blue line without touching the red lines and drag from top to bottom.

The touched part of the blue line is changed to white.

If the red line is touched, an error message is issued.

② Display



③ Terminating method

Press the Esc key to terminate and return to the Touch panel diagnostics menu.

3-8. CLERK KEY DIAGNOSTICS (European model only)

The clerk key input test is performed.

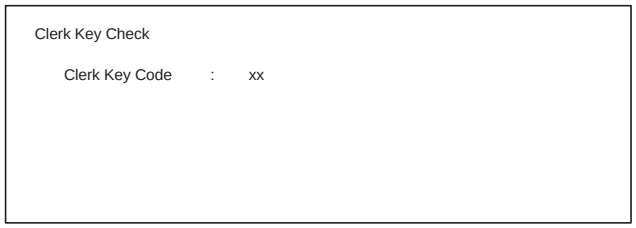
Pressing the Esc key returns to the serviceman diagnostics menu.

1) CLERK KEY CHECK

① Checking content

Key code inserted to the clerk key switch which is then displayed in a decimal value.

② Display



The clerk code is displayed at XX.

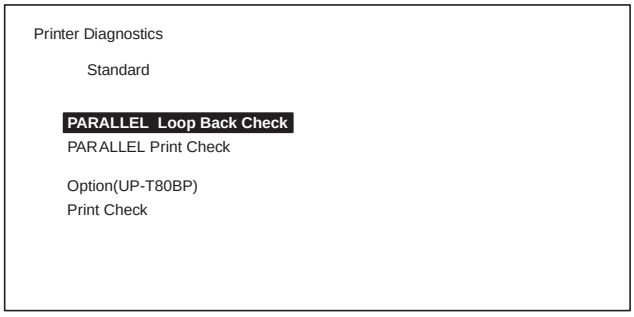
③ Terminating method.

Press the Esc key to terminate and return to the service diagnostics menu.

3-9. PRINTER DIAGNOSTICS

The parallel interface (standard) is tested.

The following menu is displayed.



The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) on the PS2 keyboard. Move the cursor to the desired item and press the Enter key to execute the selected diagnostics program.

When the selected diagnostics program is completed, the display returns to the menu screen. Pressing the Esc key returns to the service diagnostics menu.

1) PARALLEL LOOP BACK CHECK

① Checking content

To check the parallel port DSub 25 pin, use the connector (UKOG-2366BHZZ) for Parallel Loop Back Test.

Wiring is as shown below:

(D0) – (STROBE#)

(D1) – (AF#)

(D2) – (INIT#)

(D3) – (SLCTIN#)

(D4) – (ERROR#) – (SLCT)

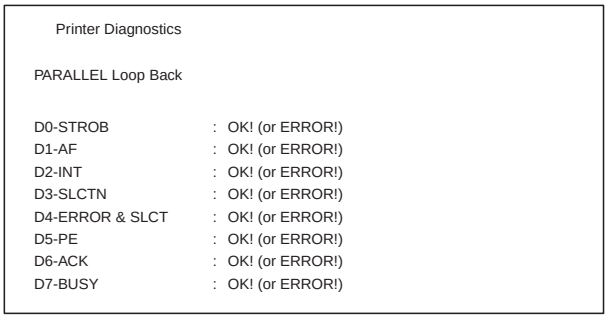
(D5) – (PE)

(D6) – (ACK#)

(D7) – (BUSY)

Perform the loop back check with the following combination of parallel ports (standard provision).

② Display



③ Terminating method.

Press the Esc key to terminate and return to the Printer diagnostics menu.

2) PARALLEL Print Check

① Checking content

The print check is performed for the standard port PARALLEL at I/O address 378H ~ 37FH. In the print check mode the D-Sub 25 pin connector is connected with a printer to allow a print pattern test.

The test procedures are as follows:

i. Data of 55H is written to I/O address 378H, and the same address is read. If the read data is not 55H, “PARALLEL Channel Disabled” is displayed and the following check is not performed.

ii. Characters of 20H ~ 7FH (ASCII code) are printed and the line is changed.
This procedure is repeated for 5 times.

② Display



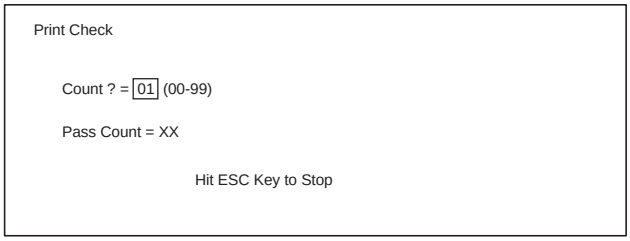
“PARALLEL Channel Disabled” is displayed only when no access to PARALLEL is allowed.

③ Terminating method.

Press the Esc key to terminate and return to the Printer diagnostics menu.

3) UP-T80BP TEST

① Display



On the above screen the setting appears in the box.

The Count can be set from “01” up to “99”. If “00” is set, printing does not stop until the ESC key is pressed.

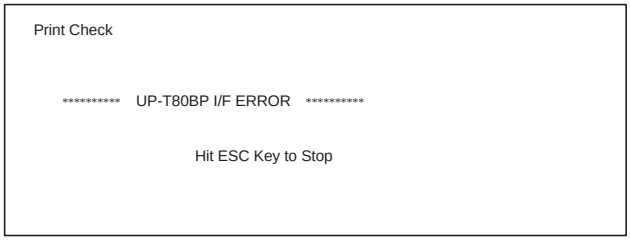
② Testing

The following patterns are printed and the paper cut command is sent by the specified number of times to the Serial output of I/O address 980H to 987H.



③ Error message

The following error message appears if a communication error occurs with the UP-T80BP.



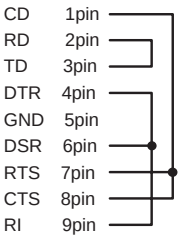
④ End of testing

The testing is finished after printing is made by the specified number of times or by pressing the ESC key.

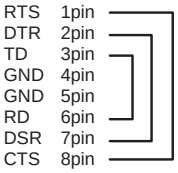
3-10. SERIAL I/O DIAGNOSTICS

The serial interface of UP-5900 is performed. To test the 9pin D-Sub port, connect the D-Sub loop back connector (UKOG-6705RCZZ).

To test the RJ45 port, connect the loop back connector (UKOG-6729BHZZ).



Loop back connector (UKOG-6705RCZZ) wiring diagram



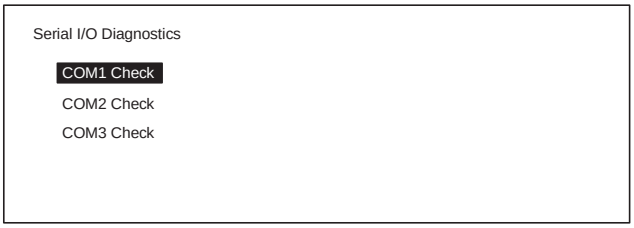
Loop back connector (UKOG-6729BHZZ) wiring diagram

The UP-5900’s 9-pin D-sub ports are used as COM1 and 2. The UP-5900 also provides a RJ45 port is used as COM3.

The following menu is displayed.

The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the PS2 keyboard. Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program.

When the selected diagnostics program is completed, the display returns to the menu screen. Pressing the Esc key returns to the service diagnostics menu.



1) COM1 CHECK

① Content

The loop back check is performed for the UART at I/O address 3F8H ~ 3FFH. The test procedures are as follows:

i. UART setting is made. If access is denied to UART at that time, “COM1 Disabled” is displayed and the following check is not performed.

ii. RTS signal is turned on/off to check that CD, CTS signal is normally operating. In case of any abnormality, ERROR is displayed.

iii. DTR signal is turned on/off to check that DSR, RI signal is normally operating. In case of any error, ERROR is displayed. When an error occurs in procedure i or ii, the following test is not performed.

iv. Set the baud rate to 19200bps asynchronous. 256 byte data of 00H ~ FFH is transmitted from SD signal. Data received at RD signal is compared to check that the both are the same. If the output data is not returned for 5 sec or more, an ERROR is displayed and the test is terminated.

v. An interruption signal is issued from UART and the number of generated interruption request signal is displayed.

② Display

```
Serial I/O COM1 Check

RTS - CD        :    PASS !!(or ERROR !!)
RTS - CTS       :    PASS !!(or ERROR !!)
DTR - DSR       :    PASS !!(or ERROR !!)
DTR - RI        :    PASS !!(or ERROR !!)
TD - RD         :    PASS !!(or ERROR !!)
INTERRUPT       :    IRQ XX
```

The number of the interruption request signal is displayed at XX.

If no access is allowed to COM1 UART, the following display is made.

```
Serial I/O COM1 Check

    COM1 Channel Disabled
```

③ Terminating method.

Press the Esc key to terminate and return to the Serial I/O diagnostics menu.

2) COM2 CHECK

① Checking content

The loop back check is performed for the UART at I/O address 2F8H ~ 2FFH. The check procedure, the display, and the terminating method are the same as COM1 Check.

3) COM3 CHECK

① Checking content

The loop back check is performed for the UART at I/O address 3E8H.

When the RJ-45 port of the UP-5900 main unit is assigned to COM3, the following points are different from COM1 Check :

① Content

- RTS-CTS is not checked.
- DTR-RI is not checked.

② Display

- RTS-CTS is not displayed.
- DTR-RI is not displayed.

COM3 is checked as well as COM1 except at the above 2 points.

3-11. LIQUID CRYSTAL DISPLAY DIAGNOSTICS

LCD test is performed.

The following patterns are displayed in sequence. Pressing the space bar proceeds to the next display. Pressing the space bar at the final pattern or pressing the Esc key during the test, will return the display to the service diagnostics menu.

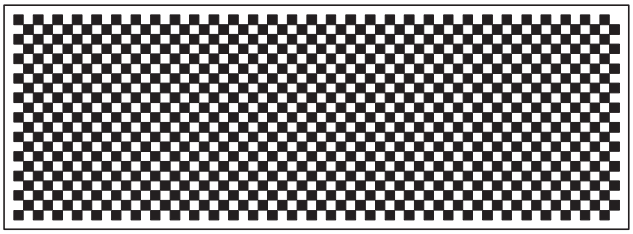
1) LIQUID CRYSTAL DISPLAY CHECK

① Checking content

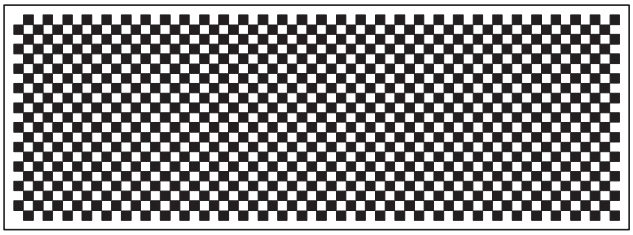
The test patterns are displayed in the following test procedures.

Pressing the space bar moves to the next pattern.

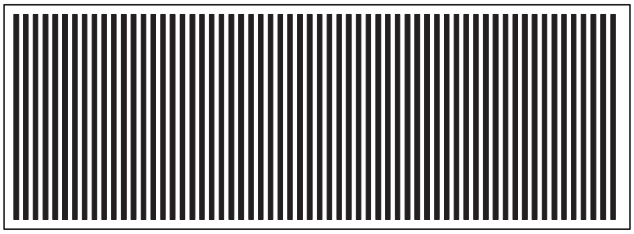
i. Black-and-white pattern in 1 dot interval



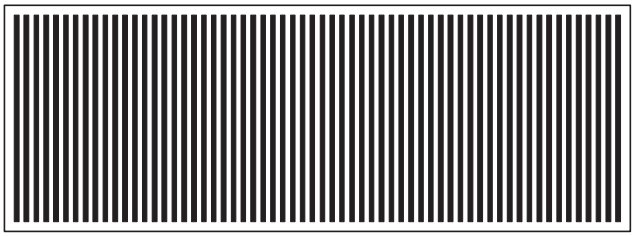
ii. Reversed pattern of pattern i.



iii. Vertical stripe pattern in 1 dot interval



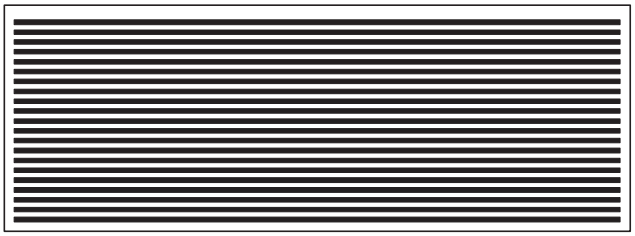
iv. Reversed pattern of pattern iii.



v. Horizontal stripe pattern in 1 dot interval

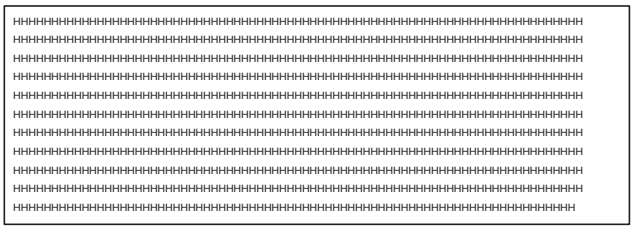


vi. Reversed pattern of pattern v.

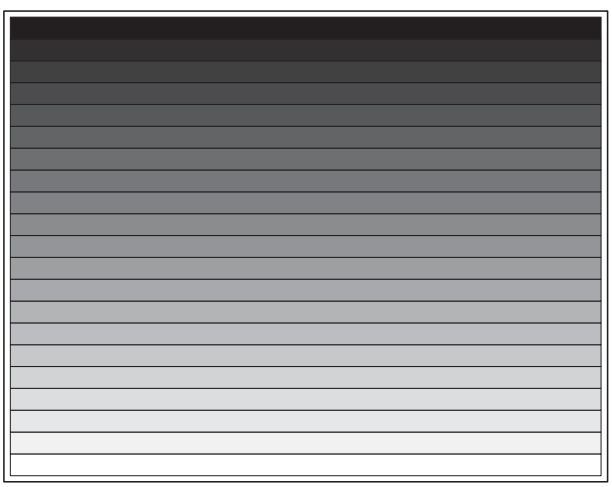


vii. “H” pattern (80 digits x 35 lines) In the 35th line, only 78 digits of “H” are displayed.

(The actual display range is 25 lines. Scroll for 10 lines to check.)



viii. Gradation pattern from black to white in 16 gradations



ix. All white pattern

x. Color bar (16 colors)

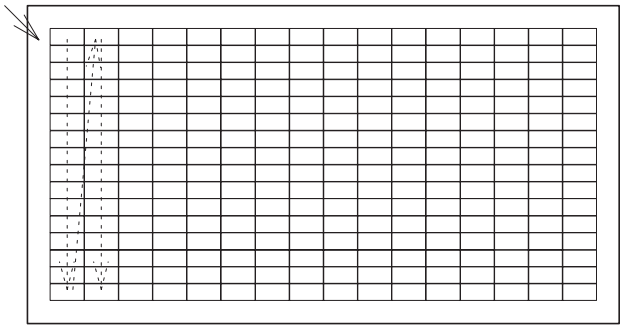
Color bars of 16 colors are displayed.



xi. Color pattern (256 colors)

Color pattern of 256 colors is displayed. The displayed colors are the default pallet.

Arrange RAMDAC register No. 0 ~ 255 from the upper left.



xii. Backlight OFF

The backlight is turned off without turning off the display.

xiii. Backlight ON

② Terminating method

Press the space bar or Esc key to terminate and return to the service diagnostics menu.

3-12. MAGNETIC CARD READER DIAGNOSTICS

This test program reads the magnetic card based on the ISO7811/1-5 standard and displays the data.

Pressing the Esc key returns to the service diagnostics menu.

1) MAGNETIC CARD READER CHECK

① Checking content

The test program reads tracks 1 and 2 of the magnetic card (UKOG-6718RCZZ) based on the ISO7811/1 ~ 5 standard, and displays the data in ASCII code. There are two kinds of data patterns to be read.

TRACK 1: IATA pattern
76 character 7bit/character (Max. 79 character)

TRACK 2: ABA data pattern
28 character, 5bit/character (Max. 40 character)

To read the card data, the following setting is performed.

- Mode set

  46h is set to PSC2 channel 1 mode set register. (IATA, 6bit)

  74h is set to PSC2 channel 2 mode set register. (ABA, 4bit)

- Start mark set

  45h is set to PSC2 channel 1 start mark register.

  0Bh is set to PSC2 channel 2 start mark register.

- Interrupt reset

  Test data is written to PSC2 channel 2 start mark register.

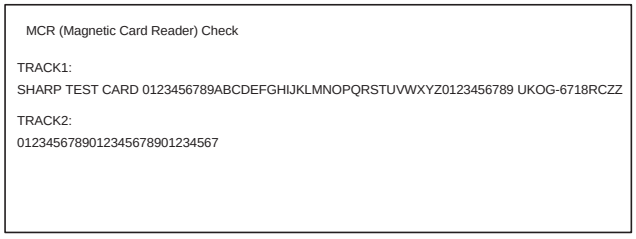
- Interrupt mask cancel 01h is written to PSC2 MCR mask register to cancel mask.

  In addition, setting for the PSC2 extension interruption is performed.

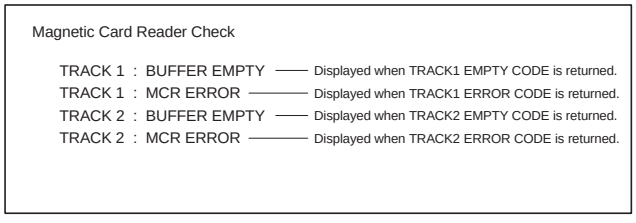
  When the card is scanned, the obtained data is written to the FIFO buffer from the start mark to LRC in sequence. Then, the card data is read by interrupt process.

  After reading data, the FIFO buffer is reset.

② Display



The above display is made when the card (UKOG6718RCZZ) is passed through the MCR. In case of an error, the error code is displayed as follows:



③ Terminating method

Press the Esc key to terminate the test and return to the service diagnostics menu.

3-13. SYSTEM SWITCH DIAGNOSTICS

The system switch information of the main PWB is displayed.

Pressing the Esc key returns to the service diagnostics menu.

1) SYSTEM SWITCH

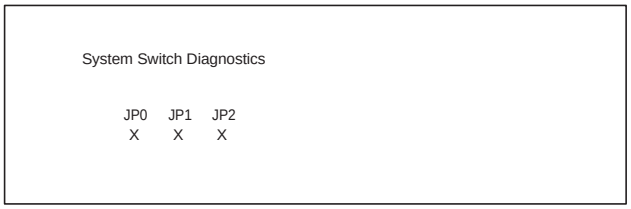
① Checking content

The system switch reads I/O address 7F0H every 10ms to display the value of bit 7, 6, 0. The relationship between the bit and JP switch is as shown in the table below.

Reference only (not for diagnostics)

Bit	7	6	0
7F0H	JP0	JP1	JP2

② Display



Each JP switch data is displayed at X. If the bit data is “1,” the display is “OFF”. If the bit data is “0,” the display is “ON”.

③ Terminating method

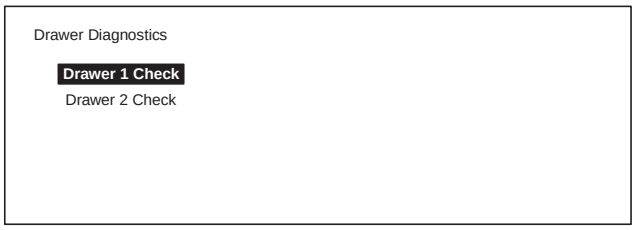
Press the Esc key to terminate the test and return to the service diagnstics menu.

3-14. DRAWER DIAGNOSTICS

The drawer open and sensor test are executed.

The following menu is displayed. The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the PS2 keyboard.

Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program. When the selected diagnostics program is completed, the display returns to the menu screen. Pressing the Esc key returns to the service diagnostics menu.



1) DRAWER 1 CHECK

① Checking content

The drawer 1 solenoid is turned on and the drawer open sensor value is sensed at every 100ms and the state is displayed.

When Drawer 1 and Drawer 2 are connected, “CLOSE” is displayed only when both the drawers are closed.

② Display

```
Drawer 1 Check

  Drawer Open Sensor  :  OPEN (or CLOSE)
```

③ Terminating method

Press the Esc key to terminate the test and return to the Drawer diagnostics menu.

Pressing the ESC again will return to the service diagnostics menu.

2) DRAWER 2 CHECK

① Checking content

Drawer 2 solenoid is turned on and the drawer open sensor value is sensed at every 100ms and the state is displayed.

When Drawer 1 and Drawer 2 are connected, “CLOSE” is displayed only when both the drawers are closed.

② Display

Same as Drawer 1.

③ Terminating method

Same as Drawer 1.

3-15. OPTION DISPLAY DIAGNOSTICS

The option display includes a microprocessor inside that allows communication with the host by RS232 conforming interface.

PSC2 UART4 is used on the main body side.

Communication conditions are as follows:

- Data length: 8 bit
- Parity (Yes/No): No
- Baud rate: 9600bps

① Checking content

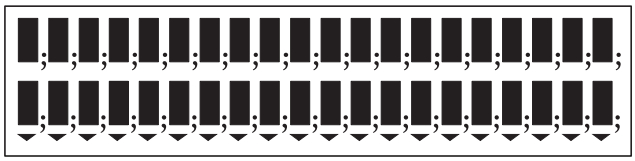
The test patterns are displayed in the sequence shown below.

Pressing the space bar moves to the next pattern.

i. The following test patterns are displayed.



ii. The test pattern with all digits ON is displayed.



iii. All OFF

② Display

```
Pole Display Check
```

③ Terminating method

Press the Esc key to turn off the VFD display and terminate the test. Return to the Option display diagnostics menu and the test is terminated.

3-16. IDE I/F & HARD DISK DIAGNOSTICS

The hard disk is tested and the information stored in the hard disk is displayed.

The following tests are executed.

- Read test: Seek (sequential, random) test, read only (target cylinder, target sector), and dump test
- Write test: Write verify test (target cylinder, target sector), and batch test.
- Other functions: Drive status display, controller check, error logging area (error information) display, and error information display

Test screen (service repair only)

```
Hard Disk Drive Diagnostics

READ MODE TEST
    Drive status display
    Sequential seek test
    Random seek test
    Seek&Read test
    Target Sector Read test
    HD Dump test
    Error LOGGING Information Display
    Disk Controller Check test

WRITE MODE TEST
    Seek&Write/Read-Verify test
    Target Sector Write/Read-Verify test
    HD Patch test
    ERROR LOGGING AREA CLEAR
    Error Table Display


 ↑ , ↓: Move ENTER : Selet ESC : Exit
```

On the above screen, select the desired test item with ↑ (UP) and ↓ (DOWN) keys and press the Enter key to execute the test.

Pressing the Esc key returns to the service diagnostics menu.

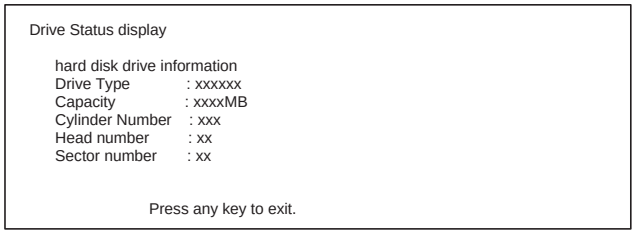
[READ MODE TEST]

1) DRIVE STATUS DISPLAY

① Checking content

The hard disk drive standard values (Memory capacity, Number of cylinders. Number of heads, and Number of sectors) are displayed.

② Display



Drive type:	Hard disk drive name
Capacity:	Hard disk memory capacity
Cylinder number:	Max. cylinder number
Head number:	Max. head number
Sector number:	Max. sector number

③ Terminating method

Press any key to terminate the test and return to the menu screen in the previous (1).

2) SEQUENTIAL SEEK TEST

[Test conditions setting]

- Cylinder Range [0 ~ inmost cylinder]
  The cylinder range to be tested is set.
- Retry Count [0 ~ 4]
  Retry count in case of an error is set.
- Error Stop/Continue/1 Pass
  Selection is made among Error Stop/Continue/1 Pass in case of an error.
- Test Start ? [Yes/No]
  Selection is made to execute the test or not.

① Checking content

In the cylinder range set above, the sequential seek is executed for every 1 track. When the seek test in the set range is completed (in the direction of 0 → inmost cylinder), it is counted as 1 pass. In case of an error during the above test, a retry is repeated up to the set number of retries. Every time an error occurs by executing retry up to the retry number and error logging is performed. Logging is made for HD and DRAM.

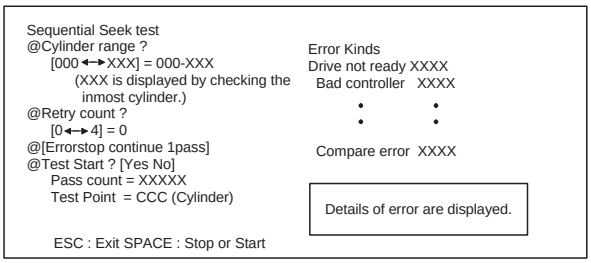
When an “Error stop” is set in the test conditions setting, and an error occurs during the above test, the error display is made and the test is stopped. Press the space bar to resume the test.

When “Continue” is set, even if an error occurs, the error display is made but the test is not stopped.

When “1 Pass” is set, a series of tests is made only once and the test is stopped.

② Display

Sequential Seek test execution screen



Select the desired items at the position of @. (@ is not displayed on the screen.)

On the above screen, when the pass count is counted up (when the point is counted up to the upper limit set in the cylinder range setting, the pass count is counted up by 1.), and if the error counter of all error items are not counted up (remaining as 00000), the test is OK.

When the space bar is pressed during the test, the test is interrupted.

When the space bar is pressed during interruption of the test, the test is started.

③ Terminating method

Press the Esc key during execution of the test or during interruption of the test to terminate the test and return to the above menu screen.

3) RANDOM SEEK TEST

[Test condition setting]

Same as the above sequential read.

However, execution of the test by 1 Pass means execution of random seek through the set cylinder range.

① Checking content

The random seek is executed for every one track in the cylinder range set previously.

When the seek test is completed in the set range, it is counted as 1 pass.

In case of an error during the above test, a retry is repeated up to the set number of retries. Every time an error occurs a retry is performed up to the set number of retries, and error logging is made. Logging is made for HD and DRAM.

When the “Error Stop” is set in the test condition setting, and an error occurs during the above test.

The error display is shown and the test is interrupted. Press the space key to resume the test.

When the “Continue” is set, even if an error occurs, the error display is made but the test is not stopped.

When “1 Pass” is set, a series of tests is made only once and the test is stopped.

② Display

Same as the above sequential read, however the following contents are different.

The test Point is changed at random in the range of 000 ~ XXX (cylinder range set value).

Each point is tested once, and the pass count is added by one with XXX times.

③ Terminating method

Press the Esc key during execution of the test or during interruption of the test to terminate the test and return to the above menu screen.

4) SEEK & READ TEST

[Test condition setting]

Same as the above sequential read. The following setting is additionally required.

- Sector count [0 ~ final sector]

The sector range to be tested is set.

① Checking content

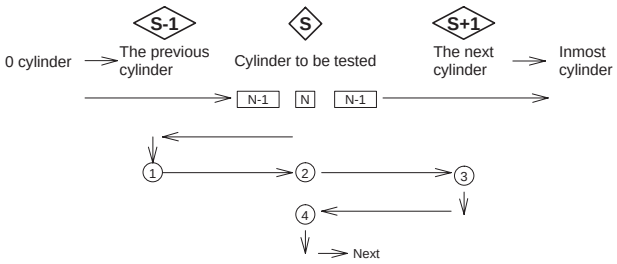
The sequential read for every one track is executed in the cylinder range and the sector range set above. (in the direction of 0 → inmost cylinder)

When the read test is completed in the set range, it is counted as 1 pass.

Before seeking, however, seek is made of the previous cylinder and the following cylinder.

(Head movement)

When track N is read, the head moves as follows:



At ② and ④, read is executed.

In case of an error during the above test, a retry is repeated up to the set number of retries. Everytime an error occurs a retry is performed up to the set number of retries and, error logging is made. Logging is made for HD and DRAM.

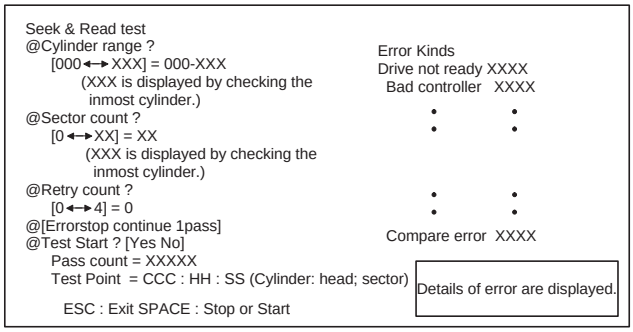
When the “Error Stop” is set in the test condition setting, and an error occurs during the above test.

The error display is shown and the test is interrupted. Press the space key to resume the test.

When the “Continue” is set, even if an error occurs, the error display is made but the test is not stopped.

When “1 Pass” is set, a series of tests is made only once and the test is stopped.

② Display



Select the desired items at the position of @. (@ is not displayed on the screen.)

(On the above screen, the thick figures are selected, and the thick figure values are selected.)

On the above screen, when the pass count is counted up (when point is counted up to the upper limit set in the cylinder range setting, the pass count is counted up by 1.), and if the error counter of all error items are not counted up (remaining as 00000), the test is OK.

③ Terminating method

The methods to interrupt, resume, and terminate the test are the same as (2) Sequential read.

5) TARGET SECTOR READ TEST

[Test conditions setting]

- Cylinder range [0 ~ inmost cylinder]
  The cylinder range to be tested is set.
- Head count [0 ~ final head]
  The head umber to be tested is set.
- Sector count [0 ~ final sector]
  The sector number to be tested is set.
- Retry count [0 ~ 4]
  Retry number incase of an error is set.
  - Error stop/Continue/1 Pass
    Selection is made among Error Stop/Continue/1 Pass in case of an error.
  - Test start ? [Yes/No]
    Selection is made between Yes/No at test start.

① Checking content

A read is made for the cylinder range, the head number, and the sector number areas set in the above.

When the read test is completed in the set range, it is counted as 1 pass.

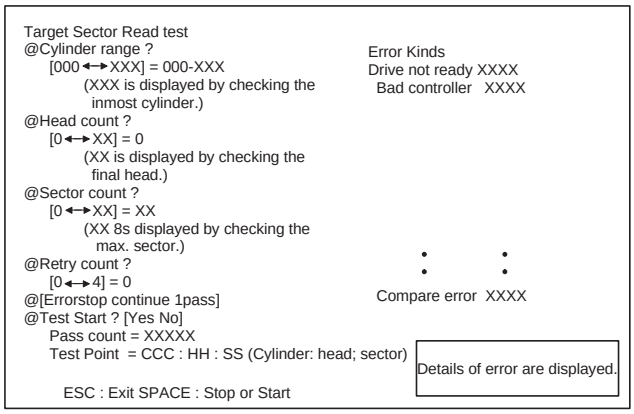
In case of an error during the above test, a retry is repeated up to the set number of retries. Every time when an error occurs a retry is performed up to the set number of retries, and error logging is made. Logging is made for HD and DRAM.

When the “Error Stop” is set in the test condition setting, and an error occurs during the above test, the error display is shown and the test is interrupted. Press the space key to resume the test.

When the “Continue” is set, even if an error occurs, the error display is made but the test is not stopped.

When “1 Pass” is set, a series of tests is made only once and the test is stopped.

② Display



Select the desired items at the position of @. (@ is not displayed on the screen.)

(On the above screen, the thick figures are selected, and the thick figure values are selected.)

On the above screen, when the pass count is counted up (when point is counted up to the upper limit set in the cylinder range setting, the pass count is counted up by 1.), and if the error counter of all error items are not counted up (remaining as 00000), the test is OK.

③ Terminating method

The methods to interrupt, resume, and terminate the test are same as (2) Sequential read.

6) HD DUMP TEST

[Test conditions setting]

- Cylinder No. [0 ~ inmost cylinder]
  A certain cylinder No. to be displayed is set.
- Head No. [0 ~ final head]
  A certain head No. to be displayed is set.
- Sector No. [1 ~ final sector]
  A certain sector No. to be displayed is set.

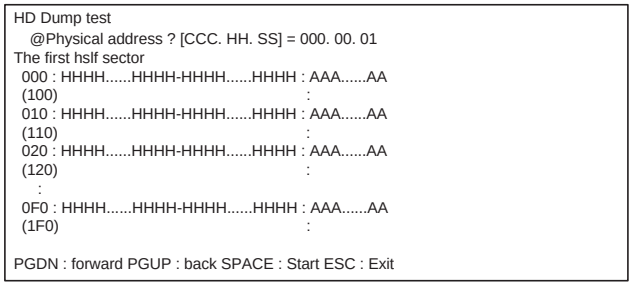
① Checking content

The sector set in the above is displayed on the screen in the unit of 256byte.

Hex data and ASCII characters are displayed.

By key operation, the following 256 bytes data or previous 256 bytes data can be displayed.

② Display



The physical address is set at the position of @. (On the above screen, the thick value is set.)

On the above screen, the first-half of 256 bytes at 000 cylinder, 00 head, and 01 sector is displayed.

Press the page down key to display the second-half of 256 bytes. (When the page down key is pressed on the above screen, the second-half of 256 bytes at 000 cylinder, 00 head, and 01 sector is displayed.)

Press the page up key to display the first-half of 256 bytes.

③ Terminating method

Press the Esc key to return to the menu screen of previous (1).

7) ERROR INFORMATION DISPLAY

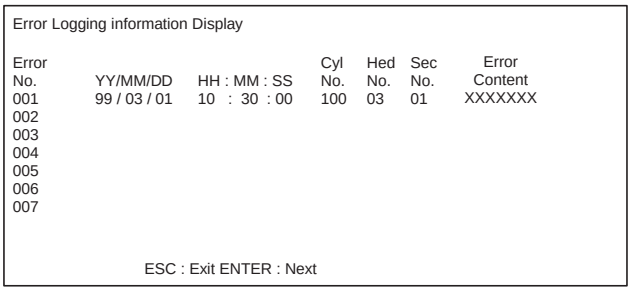
① Checking content

Error information stored in the inmost area of the HDD is displayed.

When the hard disk test is executed, error information stored in the error information storing area is displayed.

The inmost cylinder, 0 head, and 1 sector ~ 6 sector are read to be displayed.

② Display



Every time the Enter key is pressed, the next page error information is displayed.

[Descriptions on the above screen]

Error No. _____	Error information register No. (001 ~) (This is not an error code.)
YY/MM/DD_____	Year/Month/Day
HH:MM:SS _____	Hour/Minute/Second
Cylinder _____	Cylinder No.
Head No. _____	Head No.
Sec No. _____	Sector No.
Error Content _____	Error code is converted into error content and displayed.

③ Terminating method

Press the Esc key to return to the menu screen.

8) CONTROLLER CHECK TEST

① Checking content

The diagnostic command included in the F-ROM is executed to perform hard disk controller check.

② Display

```
Disk Dontroller Check test
 @[Errorstop Continue 1pass]
 @Test Start ? [Yes No]

      Pass count = XXXXX

      Controller ..... Checking

ESC : Exit SPACE : Stop or Start
```

If the section [ ] blinks and the pass count is counted up, the test is OK.

When the space bar is pressed during the test, the test is interrupted.

When the space key is pressed during interruption of the test, the test is resumed.

③ Terminating method

When the Esc key is pressed during the test or test interruption, the test is terminated and the display returns to the menu screen.

[WRITE MODE TEST]

(Note) When the following test is executed, the HDD data is destroyed.

The display shown before executing write mode test

```
When executed, Data on hard disk will be destroyed.
      Password ?  [*****]        ↑ Note message

ESC : Exit
```

Before executing the write mode test, “When executed, Data on hard disk will be destroyed.” is displayed.

Password entry is urged. Only when the correct password is entered, does the display go to the next one.

The correct password is “sharp” or “SHARP” in 5 digits. When typing the correct password, the “ ∗ “ is displayed. Instead of the character content.

9) SEEK & WRITE/READ-VERIFY TEST

[Test conditions setting]

Similar to 4) SEEK & READ TEST. Cylinder range setting is 000 ↔ inmost cylinder 2.

① Checking content

For the cylinder range and the sector range set in the above test, the worst pattern data is written sequentially for every one track.

Then, the read/verify check is made for each track.

The number of the read/verify check is one.

(Test for 1 pass)

The write is made in the direction of 0 → inmost cylinder.

The read/verify check is made in the direction of 0 → inmost cylinder.

The write is made in the direction of inmost cylinder → 0.

The read/verify check is made in the direction of inmost cylinder → 0.

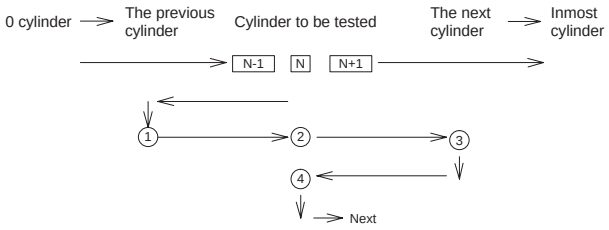
When writing data, write different data from the original stored data.

Before writing or reading, the head is moved to the previous or the following cylinder.

(Head movement)

When track N is read, the head moves as follows. (The head arm is deflected back and forth.)

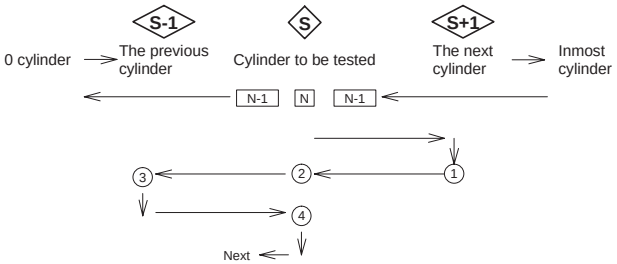
In the direction of 0 → inmost cylinder



Writing is made at ②.

Reading is made at ② and ④.

In the direction of 0 ← inmost cylinder



Writing is made at ②.

Reading is made at ②. and ④.

(Worst pattern data)

There are two kinds of worst data: B6DBH and 6DB6.

In case of an error during the above test, a retry is repeated up to the set number of retries. Every time an error occurs a retry is performed up to the set number of retries and, error logging is made. Logging is made for HD and DRAM.

When the “Error Stop” is set in the test condition setting, if an error occurs during the above test, the error display is shown and the test is interrupted. Press the space key to resume the test.

When the “Continue” is set, even if an error occurs, the error display is made but the test is not stopped.

When “1 Pass” is set, a series of tests is made only once.

② Display

Same as the previous (4). The following two points are different.

∗ Cylinder range ?

[000 ↔ XXX] (XXX is inmost cylinder 2.)

∗ Test mode: the [ ] grid is displayed.

When data writing, WRITE is displayed in the [ ] grid. When data reading, READ is displayed.

③ Terminating method

Same as (4).

10) TARGET SECTOR WRITE/READ-VERIFY TEST

[Test conditions setting]

Similar to test 5). Cylinder range setting is 000 *0* (Final cylinder 2).

① Checking content

For the cylinder range, the head number, and the sector number area set in the above, write/read/verify is made.

When the write/read test is completed in the set range, it is counted as 1 pass.

In case of an error during the above test, a retry is repeated up to the set number of retries. Everytime an error occurs a retry is performed up to the set number of retries and, error logging is made. Logging is made for HD and DRAM.

When the “Error Stop” is set in the test condition setting, if an error occurs during the above test, the error display is shown and the test is interrupted. Press the space key to resume the test.

When the “Continue” is set, even if an error occurs, the error display is made but the test is not stopped.

When “1 Pass” is set, a series of tests is made only once.

② Display

Same as the previous (6). The following two points are different.

∗ Cylinder range ?

[000 ↔ XXX] (XXX is inmost cylinder 2.)

∗ Test mode: the [ ] grid is displayed.

When data writing, WRITE is displayed in the [ ] grid. When data reading, READ is displayed.

③ Terminating method

Same as test 5).

11) HD PATCH TEST (UTILITY)

[Test conditions setting]

Similar to the previous 6). The cylinder range setting is 000 ↔ (Final cylinder 2).

① Checking content

The sector set in the above is displayed on the screen in the unit of 256 bytes.

Hex data and ASCII characters are displayed.

By key operation, the following 256 bytes data or previous 256 bytes data can be displayed.

After changing data on the screen, data is written to the selected set position.

② Display

Similar to test 6). Data in the HDD can be patched.

Patching is made as follows:

To patch data in the HD, change data on the screen.

(Move the cursor with ↑ , ↓ , ←, →, keys and enter data with 0 ~ F key.

Then select “Yes” in “Up data ? [Yes/No]” and press Enter key.

(Move with ← key.)

With the above procedure, patch is made.

③ Terminating method

Same as test 6).

12) ERROR LOGGING AREA CLEAR

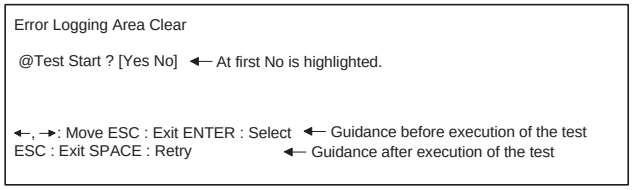
① Checking content

The last cylinder area in the HD is cleared with 00H.

(Error logging area: last cylinder, all sectors of 0 head)

The areas to be cleared with 00H is the last cylinder and all the sectors of 0 head.

② Display



Select “Yes” at position @ (move with the ← key) and press the Enter key to execute the test.

When the test is executed once, the mode enters the key waiting mode. After executing the test, press the space key to execute again.

③ Terminating method

Press the Esc key to return to the menu screen.

13) ERROR TABLE DISPLAY

When an error occurs during the above test, error information is stored in the DRAM and the content is displayed.

If there is no error, OK or NO ERROR is displayed.

14) SUPPLEMENTAL ITEMS

Error information is stored up to 44 items in the sequence of occurrence from when the function is selected. If the item number exceeds 44, the error information is not stored any more.

15) ERROR CONTENT

The following error content is error information directly obtained from the HDD controller.

[Error code and meaning]

Error code	Error message
0	OK (This message is displayed when the test is normally completed.)
1	Drive not ready (HDD is not ready. STATUS REG bit 6 : 0)
2	Bad controller (HDD controller abnormality,diag status error STATUS REG bits : 1 or DIAG STATUS >= 2)
3	Track 000 Error (TRACK 000 cannot be found with RESTORE command. ERROR REG bit 1 : 1)
4	Seek Error (A seek error occurs. After STATUS COMMAND is executed,STATUS REG bit 4 : 0)
5	ID not Found (ID field is not detected. ERROR REG bit 4 : 0)
6	Data Address Mark not Found (Data Address Mark is not found. ERROR REG bit 0 : 1)
7	Bad Block Detect (BAD block mark is stored in the ID field of request sector. ERROR REG bit 7 : 1)
8	Uncorrectable error (An uncorrectable read error occurs. ERROR REG bit 6 : 1)
9	Others error (The other error STATUS REG bit 0 : 1,and ERROR REG : 0)
10	Time out error (Time out occurs when making access to HDD.)
11	Compare error (The written data and the read data are not the same.)

16) ERROR INFORMATION STORING AREA

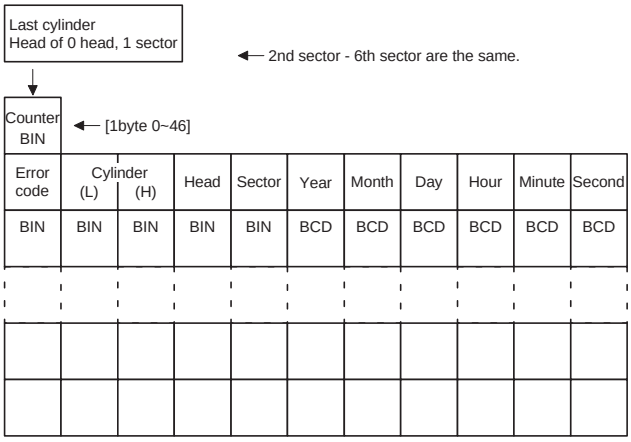
① Error information storing area for diagnostics

1 sector ~ 6 sector of 0 head of the last cylinder is used.

Used in the following format from the head of each sector.

(Error information format for every sector)

1 + 46 x 11 = 507 bytes is used in one sector.



Error code	Cylinder (L)	Cylinder (H)	Head	Sector	Year	Month	Day	Hour	Minute	Second
BIN	BIN	BIN	BIN	BIN	BCD	BCD	BCD	BCD	BCD	BCD

3-17. FDD DIAGNOSTICS

This is a test program that checks the floppy disk drives.

(Do not execute this program after performing a D-RAM test.)

1) FDD CHECK

① Description

A test file is opened on a floppy disk and data (256 bytes) of 00h - FFh is written four times on the disk before read and verification are performed.

② Display

After making sure the screen looks like this, insert a formatted FD (W/R-TEST disk) into the drive and press any key.

```
Please insert W/R-TEST disk to drive A:

Warning
Data in the disk A: will be destroyed.
```

Note: W/R-TEST disk: Formatted FD (Turn off write-protection)

The screen looks like this during testing.

```
FDD Write/Read & Compare Check
```

③ Error

When an error occurs, the following message appears on screen.

```
**********
**********  FDD ERROR !!!  **********
Drive not ready
```

Note: An error message appears at the hatched area

Error message	Description
Drive not ready	No FD in drive
Verify error	Write data is different from Read data
Write protect error	Disk is write-protected.
General failure	FD is not formatted or others
No space left on device	No disk space available

Other than the above messages, some MS-DOS error messages may be displayed.

④ Terminating testing

When the screen displays the following message, remove the FD and press any key.

```
Please out W/R-TEST disk from drive A:
```

3-18. FAN & LCD ON/OFF DIAGNOSTICS

1) FAN & LCD ON/OFF CHECK

① Checking content

The CPU, the fan, the exhaust fan and the LCD are turned ON/OFF. When this menu is selected, the following display is shown.

```
FAN&LCD ON/OFF Diagnostics

HIT ANY KEY
```

When any key is pressed, the CPU fan and the exhaust fan are stopped and the LCD and the backlight are turned off.

When any key is pressed under this state, or if there is no key input for 10 sec, the display automatically returns to the main menu and the test is terminated.

3-19. POWER HOLD DIAGNASTICS

1) POWER HOLD CHECK

① Checking content

Two types of states such as power hold and power switch are displayed.

```
Power  Hold Diagnostics
       Power Hold      :<~>ON (or OFF)
       Power Switch    :<~>ON (or OFF)
```

When pressing the space key, power hold is switched between ON and OFF.

3-20. OPERATING PROCEDURE OF LAN INTERFACE DIAGNOSTICS

■Diagnostic program: creating an MS-DOS starting media (FD)

Before executing the Diagnostic program, create the MS DOS starting media and copy the Diagnostics program onto it.

How to create an MS DOS starting media

1) Execute the command given below on the PC where the MS-DOS Ver. 6.22 is running and create an MS-DOS starting media (FD).

2) Copy the Diagnostics program onto the MS-DOS starting media (FD).

1) GENERAL

This Diagnostic program, "RSET8139.exe" is a general-purpose program on MS-DOS for the LAN controller, RTL8139C (made by Real Tek: http://www.realtek.com.tw) used in the UP-5900 series.
"PG8139.EXE" is a tool to set the MAC address of the above LAN controller.
The operating procedures of "RSET8139.exe" (Ver. 5.01) and "PG8139.EXE" (Ver. 5.05) are described below.
How to obtain the program is shown in Real Tek's web site (http://www.realtek.com.tw).

2) SYSTEM CONFIGURATION

The system requires the pos terminal, and a PS2 keyboard for diagnostic operations.

3) LAN INTERFACE DIAGNOSTICS

■LAN DIAGNOSTICS (RSET8139.EXE) GETTING STARTED

Getting Started:

Excute “RSET8139.EXE“ by entering the command with the PS2 keyboard as follows:

A: \ >RSET8139

“A: \ >” is the DOS prompt. (Used by the FD)

∗Do not load any device drivers when using this program.

∗To operate other applications after performing this program, re-boot the machine.

■SELECTION MENU

The Diagnostics menu is started and the following menu is displayed.
The high lighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the PS2 keyboard.
Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program.

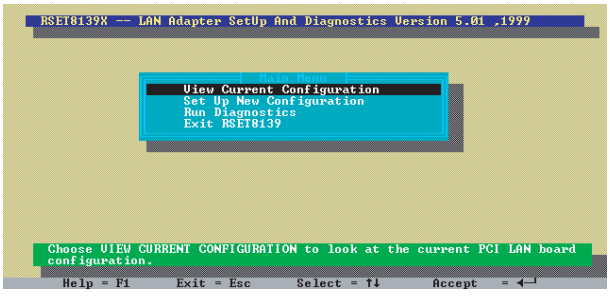


Fig. 1

■DIAGNOSTICS ON BOARD

This program is used to check the LAN functions on stand-alone UP-5900.
For execution, use the cursor key (UP ↑ and DOWN ↓) and Enter key to select "Run Diagnostics" → "Run Diagnostics On Board" on the main menu.

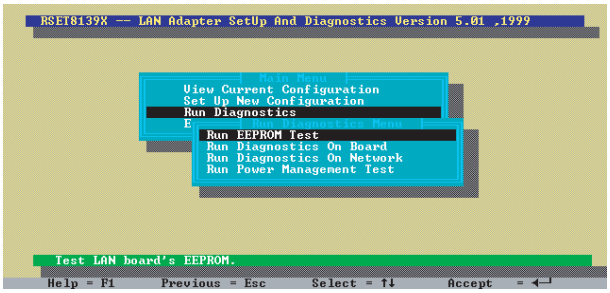


Fig. 2

① Display

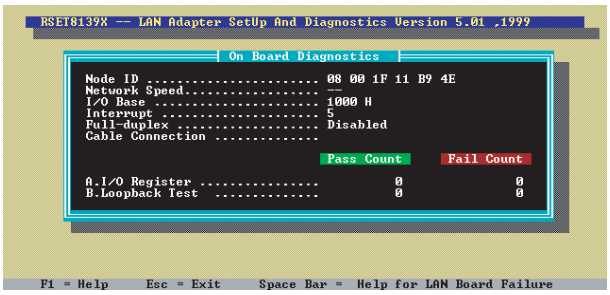


Fig. 3

② Checking Content

- Node ID

The individual Node ID (MAC address) of each UP-5900 is displayed.

IN the UP-5900, the seal indicating the lower 6 digits (08 00 1F) of the MAC address is attached to the position shown in the figure below on the main PWB.

If a MAC address different from that indicated on the seal is displayed, check the following possible cause i ~ iii:
Refer to item 4 and correct the MAC address properly.

i. EEPROM abnormality
ii. Written MAC address is erroneous.
iii. No MAC address is written.

- I/O Register, Loop back test

If the UP-5900 LAN functions are proper, the pass count of the function test counts up.

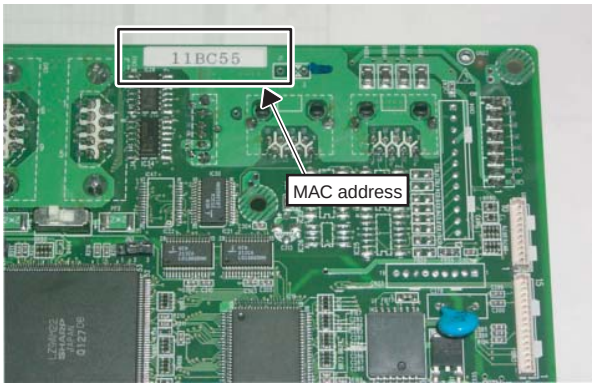


Fig. 4

■DIAGNOSTICS ON NETWORK

This program is used to check the LAN communication function with two units of the UP-5900.
For checking, a cross cable of UTP enhanced category 5 is required as well as two units of the UP-5900.

For execution, use the cursor key (UP ↑ and DOWN ↓) and Enter key to select "Run Diagnostics" → "Run Diagnostics On Network" on the main menu.

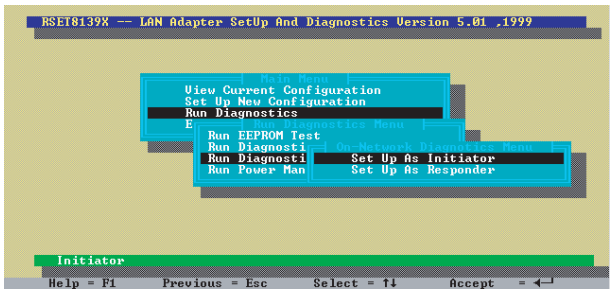


Fig. 5

In Diagnostics On Network, one unit of the UP-5900 is set as the initiator and the other as the responder. To execute the program, execute "Set Up As Responder" on the main menu of the responder unit before executing "Set up As Initiator" on the main menu of the initiator unit.

When the LAN functions of the units and the cable connection are proper, the initiator unit displays "Packet Transmitted OK" and the counter of "Packet Received OK" counts up. On the other hand, "Tk OK" and "Rx OK" counters of the responder unit count up.

4) MAC ADDRESS WRITING PROCEDURE

■ MAC ADDRESS WRITING TOOL (PG8139.EXE) EXECUTION ENVIRONMENT

To set the MAC address of the UP-5900, "PG8139.EXE" and "8139C.CFG" (configuration file) are required.

The MAC address must be written after "NoteID=" on the first line of "8139C.CFG" by using a text editor.

The lower 6 digits of the MAC address is indicated on the seal attached as shown in Fig. 4. The upper 6 digits (08 00 1F) is common to all the units.

∗Do not load any device drivers when using this program.

∗To operate other application after performing this program, re-boot the machine.

The first line to the third line of 8139C.CFG

```
NodeID = 08 00 1F 11 B9 4E      ;Note: Leave at least one blank space between
VID = 10 EC                     ;Vendor ID
DID = 81 39                     ;Device ID
 .
 .
 .
```

Fig. 6

■ MAC ADDRESS WRITING TOOL (PG8139.EXE) EXECUTION PROCESS

Place PG8139.EXE and 8139C.CFG in a same directory. Type "PG8139.EXE/pci" to execute the program. If the program is properly executed, the following display of execution is shown.

"NodeID" in 8139C.CFG is automatically incremented every time when the program is executed. When, therefore, "PG8139.EXE/pci" is executed again, "08 00 1F 11 89 4F" is displayed.

Display of execution

```
A: \>PG8139 /PCI

This is Mechanism One PCI system.

IOBASE = 1000,  IRQ = 05

 EEPROM Version 5.05


Programming EEPROM is successful!!!
NodeID = 08 00 1F 11 B9 4E
**8139C(PCI) EEPROM map **
```

Fig. 7

CHAPTER 5. CIRCUIT DESCRIPTION

1. OUTLINES

1-1. COMPOSITION

(1) CPU <Intel: Celeron>

Core Frequency: 566MHz
Front Side Bus Frequency: 66.66MHz
L1 Cache: 32kbyte (Instruction: 16kbyte, Data: 16kbyte)
L2 Cache: 128kbyte (on die)
64-bit Data Bus
Power Supply: Core voltage = 1.7V; I/O voltage = 2.5V; GTL+ voltage = 1.5V

(2) Chipset

North Bridge: <Intel: 440BX (82443BX Host Bridge/ Controller)>
Processor/Host Bus Support: GTL+ bus driver
Integrated DRAM controller: 64-bit data interface with ECC support (SDRAM only)
PCI Bus Interface: PCI Clock = FSB Clock /2
AGP Interface: AGP-66/133 3.3V device support
Power Management Function: Not Used
South Bridge: <Intel: PIIX4e (82371EB)>
Multifunction PCI to ISA Bridge:
Power Management Logic: Not Used
Integrated IDE Controller: Supports “Ultra DMA”
Enhanced DMA Controllers: 82C37 ×2
Interrupt Controller: 82C59 ×2
Interval Timer: 82C54
Universal Serial Bus: USBv1.0 ×2 (Use 1 port)
SM Bus Support:
Real Time Clock: 256byte Battery Back-up CMOS SRAM

(3) Graphics Controller <SMI: Lynx3DM4+>

AGP & PCI Interface: Use AGP ×1
Video memory: 4Mbyte
Display Support: DSTN and TFT panel support up to 1280 × 1024 (SXGA)

(4) Ultra I/O <NS: PC87309>

FDC: Enable
Serial Port: 16C550 compatible with Infrared ×2
Parallel: used for LPT1

(5) POS System Controller <SHARP: PSC2 (LZ9AM22)>

BIOS ROM Bank Control: Fixed 2 banks
UART ×5: 8250 compatible COM 5ch
Clocked Serial I/O ×2: CKDC I/F
Mode Switch Sense: 16 bits (Not Use)
Clerk Switch Sense: 16 bits
MCR Interface: 2 tracks
Drawer Interface: 4 Drawers (Use 2 Drawers)

(6) PS/2 Keyboard Controller KBC <Mitsubishi: M38813M010>

Full Keyboard control
Mouse Control
Matrix Key Control: used for Option POS key Pad

(7) Clock Generator <ICS: ICS9248-39>

(8) Memory <PC-100 or Higher>

Standard Memory: SDRAM 128Mbyte
Option Memory: 168pin DIMM socket ×1 (Max 128Mbyte, Total 256Mbyte)
(ECC Support)
BIOS ROM: 512kbyte Flash ROM

(9) Serial Ports

Serial1 (used for COM1): Ci/+5V switchable - DSUB9 with FIFO (by Ultra I/O)
Serial2 (used for COM2): Ci/+5V switchable - DSUB9 with FIFO (by Ultra I/O)
Serial3 (used for COM3/5): SG/+5V Pattern Cut & Jumper - RJ45 without FIFO (by PSC2)
Serial4: RJ45 without FIFO (by PSC2) (Not Use)
Serial5: used for Built-in Printer - TTL level interface
Serial6: used for Customer VFD control - RJ45 (for UP-P20DP) or 7pin CN(for UP-I20DP)
Serial7: used for Touch Panel control - TTL level interface

(10) Analog Touch Panel <Fujitsu: 12.1 inch>

Controller: Fujitsu N010-0559-V021
Panel: Fujitsu N010-0550-T721
Resolution: 1024 × 1024

(11) LCD <HannStar HSD121PX11-A> <Hynics HT12X11>

12.1 inch TFT 1024 × 768 × 16bit color

(12) Hard Disk Drive <Fujitsu MHN2150AT>

Capacity: 15Gbyte(Pending)

(13) Floppy Disk Drive <SAMSUNG SFD-321B>

2 Mode (2MB/1M) Disk Drive

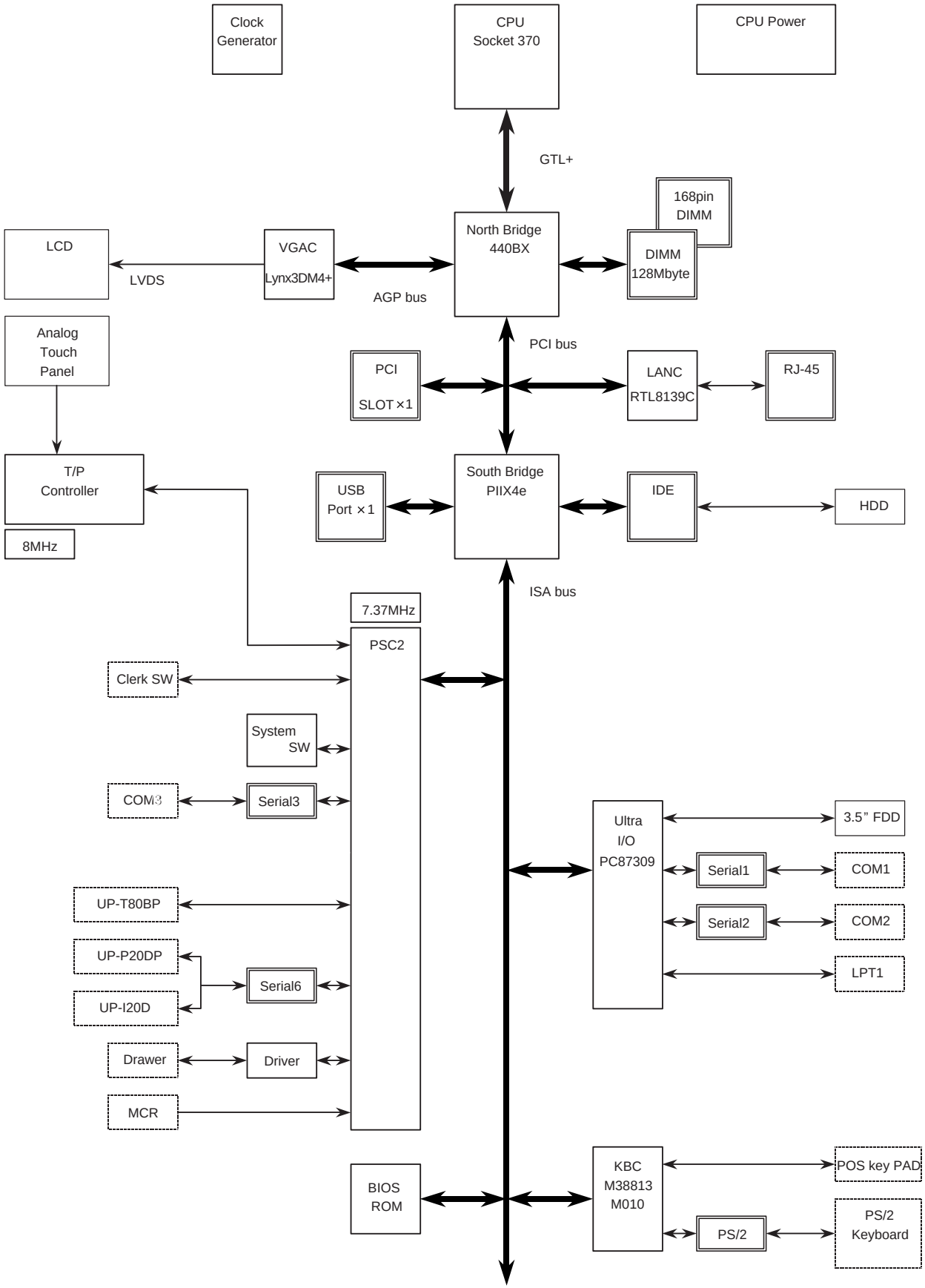
(14) LAN Controller <RealTek: RTL8139C>

10base-T/100base-TX

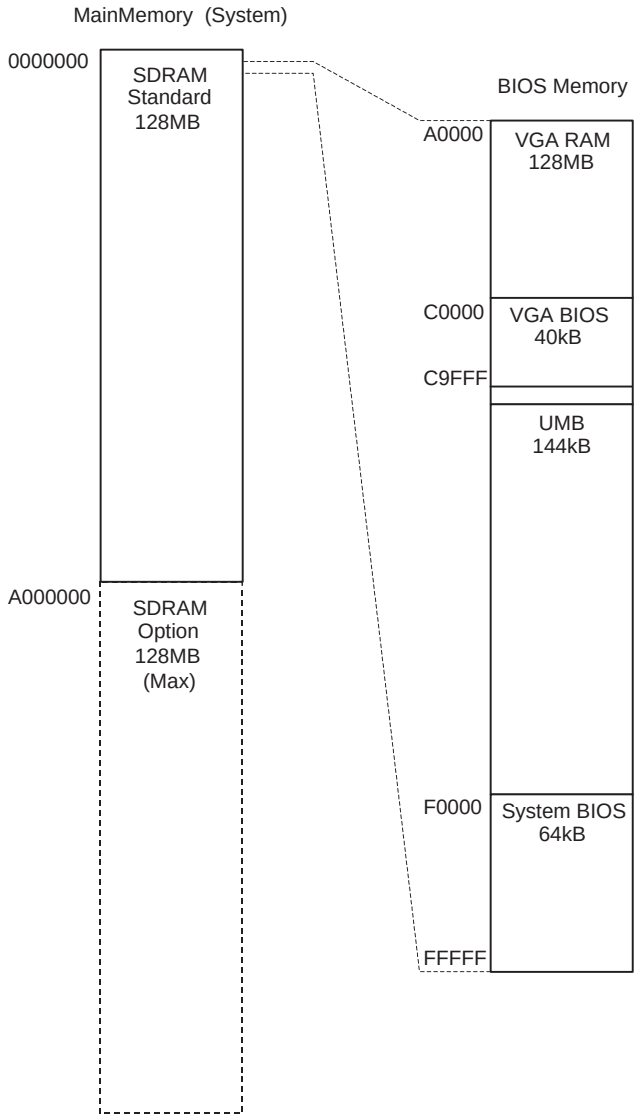
1-2. PERIPHERALS

Item	Model Name	Specification
Customer Display	UP-I20DP	2 line 20 digits dot display Mounted in the cabinet
Customer Pole Display	UP-P20DP	2 line 20 digits dot display External Pole Display
Magnetic Card Reader	UP-E12MR2	For ISO 1&2 stripe card Mounted on the cabinet
Remote Drawer	ER-03DW	
	ER-04DW	
Built-in Printer	UP-T80BP	1 station 80mm width thermal printer Mounted in the cabinet
Receipt & Journal Printer	ER-01PU	2 station (Receipt/Journal) printer
Hand Scanner	ER-A6HS1	For reading Bar code
POS Key Pad	UP-C30PK	Raised key 27 keys (std.), 30 keys (max.)

2. BLOCK DIAGRAM



3. MEMORY MAP



4. I/O ADDRESS MAP

4-1. PC SPECIFICATION

Address	Standard I/O [Option I/O]	Address	Legacy ISA I/O
00-0F	DMA ch0-3 control	400-40A	
10-1F	(System)	40B	EISA DMA Extended Mode control
20-21	Master 8259 Interrupt control	410-4EF	
22-24	Chipset Configuration	4D6	EISA DMA Extended Mode control
40-43	Timer control	4D7-57F	
48-4B	(Timer control)	580-59F	POS I/O
50-52	(System)	5A0-7EF	
60-6F	Keyboard/Mouse control	7F0-7F1	PSC Special System Register
70-7F	RTC/CMOS RAM Index/Data	7F2-7FF	
80-8F	DMA Page Register	800-97F	
90-9F	System Port A Register (PS/2 port)	980-99F	POS I/O
A0-A1	Slave 8259 Interrupt control	9A0-A78	

Address	Standard I/O [Option I/O]
C0-DE	DMA ch4-7 control
F0-F1	(Coprocessor busy clear/reset)
102	65550 (VGAC) Global Enable Register
110-16F	
170-177	Secondary IDE control
180-19F	POS I/O
1A0-1EF	
1F0-1F7	Primary IDE control
200-26F	
278-27F	[Parallel Port 2 (LPT2) control]
280-2DF	
2E8-2EF	COM4 control
2F0-2F7	
2F8-2FF	COM2 control
300-36F	
378-37F	Parallel Port 1 (LPT1) control
380-38F	
398	Super I/O Configuration Port
3A0-3AF	
3BC-3BF	[Parallel Port 3 (LPT3) control]
3C0-3DF	EGA/VGA control
3E5	[BIOS ROM Write Control]
3E8-3EF	COM3 control
3F0-3F7	FD/HD control
3F8-3FF	COM1 control

Address	Legacy ISA I/O
A79	[PnP ISA Auto Configuration Port]
A7A-BFF	
C00-CF7	
CF8-CFF	PCI Configuration
D00-D7F	
D80-D9F	Reserved[POS I/O]
DA0-FFF	
DA0-FFF	

4-2. POS SPECIFICATION

Address	POS I/O	
180-189	Extended Interrupt control	O
18A	Drawer control	O
18B-18F	Timer Counter control	O
190-191	CSIO1 (CKDC) control	RSVD
192-193	CSIO2 (CKDC) control	RSVD
194	BIOS Bank control	O
195	ROM & RAM Disk Base Address	RSVD
196-197	Interrupt Status Read	O
198-199	Mask/Flash ROM Bank control	RSVD
19A-19B	PS-RAM Bank control	RSVD
19C-19D	Mode Switch	RSVD
19E-19F	Clerk Switch	O
580-585	MCR control	O
588	General Purpose I/O	O
590-597	COM5 (Serial3) control	O
598-59F	COM6 (Serial4) control	RSVD
980-987	Serial5 (Built-in Printer)	O
988-98F	Serial6 (CU.VFD) control	O
990-997	erial7 (Touch Panel) control	O
D80-D8F	[Option]	
D90-D9F	[Option]	

5. DMA CHANNEL MAPPING

DMA Channel	Legacy ISA DMA function
0	—
1	—
2	Floppy Disk Controller
3	ECP parallel port on LPT1
4	[Cascade]
5	—
6	—
7	—

6. INTERRUPT

6-1. IRQ MAPPING

Master 8259	Slave 8259	Fixed ISA Default	Power On Default	Available Device	UP-5900 Recommended
IRQ0		System timer	Timer	Timer	Timer
IRQ1		Keyboard	KBC	KBC	KBC
IRQ2		PIC cascade	(Cascade)	(Cascade)	×
	IRQ8	RTC/CMOS	RTC/CMOS	RTC/COMS	RTC/CMOS
	IRQ9	—	IRQx	IRQx	IRQx
	IRQ10	(COM4)	ISA/Serial4	Serial4/3/7 / ISA	Serial4 †
	IRQ11	(COM3)	ISA/Serial3	Serial3/4/7 / ISA	Serial3
	IRQ12	Mouse	PCI/(ISA)/[KBC]	PCI/(ISA)/[KBC]	PCI
	IRQ13	Coprocessor	×	×	×
	IRQ14	Primary IDE	HDC	HDC	HDC
	IRQ15	Secondary IDE	Serial7	Serial7/3/4 / IRQx	Touch Panel
IRQ3		COM2	Serial2	Serial2	COM2
		COM4	×/Serial4	×/Serial4	×
IRQ4		COM1	Serial1	Serial1	COM1
		COM3	×/Serial3	×/Serial3	×
IRQ5		(LPT2)	ISA	ISA	PCI
IRQ6		FDC	FDC	FDC	FDC
IRQ7		LPT1	LPT1	LPT1	LPT1

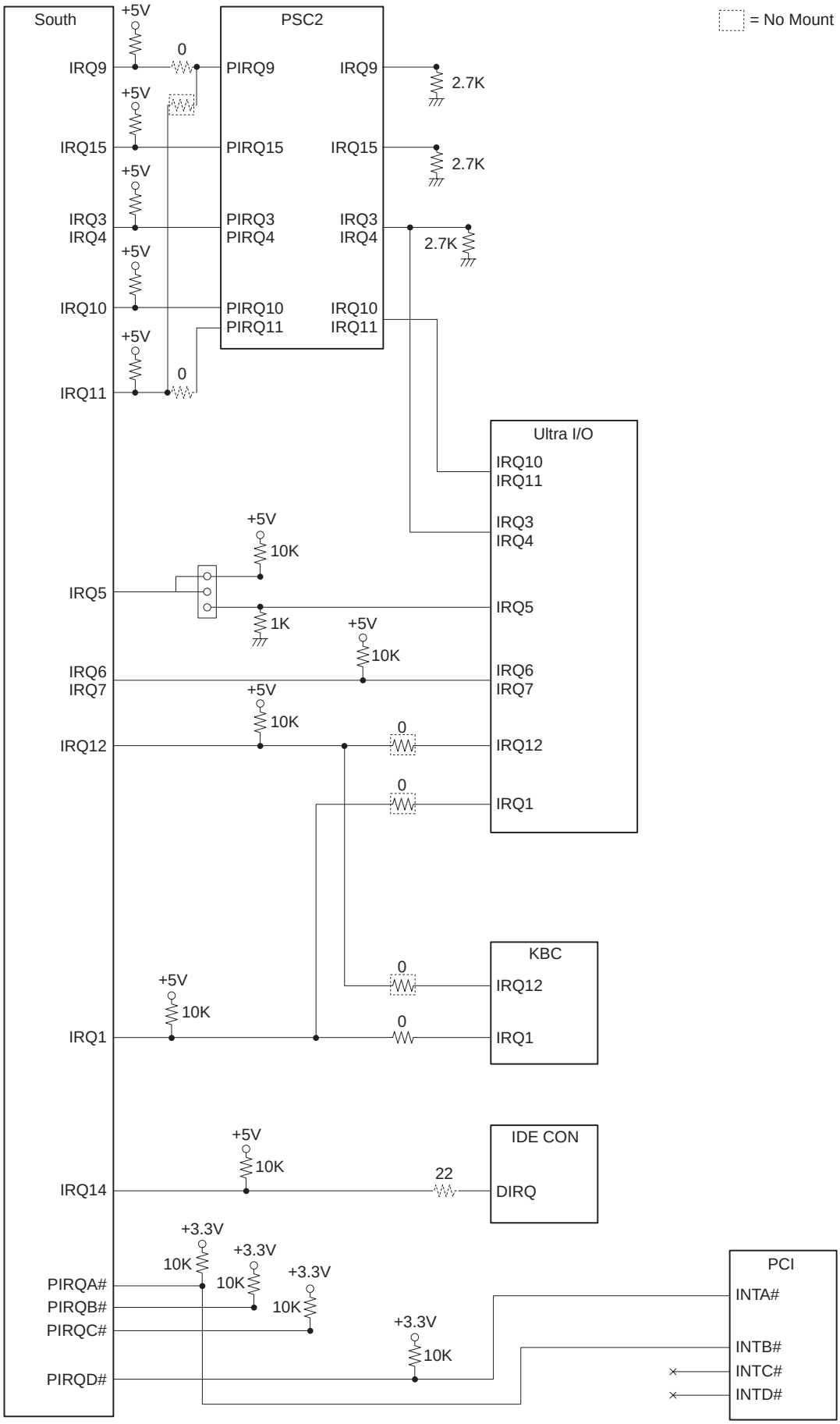
† = No Using

[ ] = This function is used with 0ohm Resistor, etc.

Extended Interrupt	On-Board POS Device	
IRQx0	MCR	For UP-E12MR/E12MR2/J12MR2
IRQx1	Serial5 [Built-in Printer]	For UP-T80BP
IRQx2	Serial6 [VFD]	For UP-P20DP/I20DP
IRQx3	POS Key	(BE-8500)
IRQx4	CSIO1 I/F	For POS key I/F(BE-8500)
IRQx5	CSIO2 I/F	For ER-A8DP(UP-5700)
IRQx6	FROM Busy	
IRQx7	POFF	
IRQx8	SINT0	
IRQx9	Reserved [Mode Switch]	not use
IRQx10	TC0OVF	
IRQx11	TC0CMP	
IRQx12	TC1CMP	
IRQx13	Serial4 (COM6)	Reserved
IRQx14	Serial3 (COM5)	
IRQx15	Clerk Switch	Only for V Model

- IRQ9 (SCI) is assigned for interruption of POS Device, and does not support ACPI.
- IRQ10 is reserved for interruption of Serial4.

6-2. IRQ BLOCK CHART



7. PCI BUS

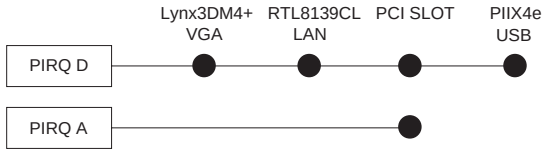
7-1. DEVICE NUMBER DECODE

Bus	Device Number	Func	IDSEL	Device	Remark
0	0000h	0000h	AD11	440BX	Host to PCI Bridge
	0001h	0000h	AD12		PCI to PCI Bridge
	0007h	0000h	AD18	PIIX4e	PCI to ISA Bridge
		0001h			IDE Interface
		0002h			USB Interface
		0003h			Power Management
	000Ah	0000h	AD21	RTL8139C	LAN Controller
	0012h	XXXXh	AD29	PCI SLOT	Expansion SLOT
1	0000h	0000h	AD16	Lynx3DM4+	VGA (AGP connection)

7-2. BUS ARBITRATION

Master Device No.	Request allow signal	Device
Device 0	REQ0#, GNT0#	(Not Used)
Device 1	REQ1#, GNT1#	(Not Used)
Device 2	REQ2#, GNT2#	(Not Used)
Device 3	REQ3#, GNT3#	PCI Slot

7-3. INTERRUPT REQUEST



PIRQ D is connected to the above PCI device and PCIIRQ0 of PCI SLOT, and connected to IRQ2 by BIOS.
PIRQ A is connected to PCIIRQ1 of PCI SLOT, and connected to IRQ5 by BIOS.

Interrupt requests which can be used with PCI slot are limited to INTA# (PCI) and INTB# (PCI). INTC# (PCI) and INTD# (PCI) must not be used.

PCI Interrupt SelectionPIO

PIO PCIIRQ	Selection	PCI Interrupt
PIO PCIIRQ0#	IRQ12	INTA#
PIO PCIIRQ1#	IRQ5	INTB#
PIO PCIIRQ2#	Disable	INTC#
PIO PCIIRQ3#	Disable	INTD#

8. SM BUS

Address	Device	Remark
10100000b	DIMM 0	UP-5900 standard memory supports SPD.
10100010b	DIMM 1	DIMM can be set with SPD.
00110000b	LM84CIM	CPU Temperature SENSOR
11010010b	ICS9248	Clock Generator

9. CPU

Intel's embedded Celeron (RB80526RX566128SL4PC) is used.
The clock frequency of CPU is automatically multiplied in the Chip.

System Bus, Core Frequency

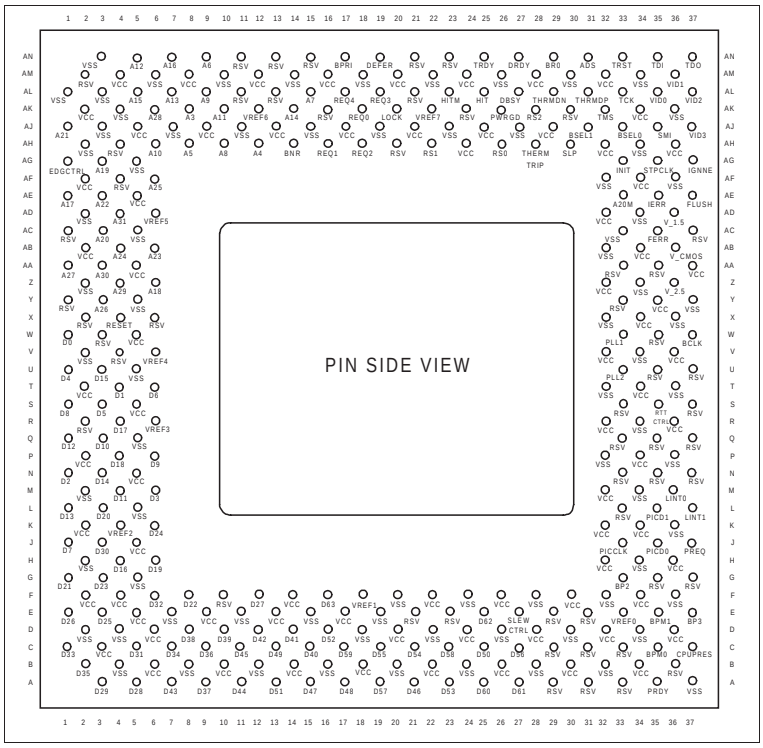
Core Frequency (MHz)	BCLK Frequency (MHz)	Frequency Multiplier
566	66	8.5

The core voltage of CPU is automatically set by connecting the VID terminal to the power IC.

Voltage Identification Definition

VID3	VID2	VID1	VID0	VccCore	Celeron566
0	1	1	1	1.70	Step C

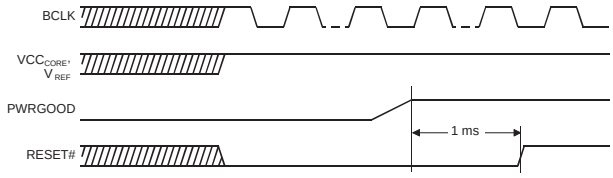
9-1. PIN ASSIGNMENTS



9-2. PIN DISCRIPTION

Signal	Type	Description
A[31:3]#	I/O	The A[31:3]# (Address) signals define a 2^{32}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel Celeron processor system bus. The A[31:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[31:3]# pins to determine their power-on configuration.
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the Intel Celeron processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[31:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
BCLK	I	The BCLK (Bus Clock) signal determines the bus frequency. All Intel Celeron processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.
BNR#	I/O	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all Intel Celeron processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.
BPRI#	I	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the Intel Celeron processor system bus. It must connect the appropriate pins of all Intel Celeron processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>BSEL[1:0]</td><td>I/O</td><td>These signals are used to select the system bus frequency. The frequency is determined by the processor(s), chipset, and frequency synthesizer capabilities. All system bus agents must operate at the same frequency Individual processors will only operate at their specified front side bus (FSB) frequency. On motherboards which support operation at either 66 MHz or 100 MHz, a BSEL[1:0] = “x1” will select a 100 MHz system bus frequency and a BSEL[1:0] = “x0” will select a 66 MHz system bus frequency.
These signals must be pulled up to 2.5V or 3.3 V with 1 KΩ resistor and provided as a frequency selection signal to the clock driver/synthesizer.
note: BSEL1 is not used by the Celeron processor.</td></tr>
<tr><td>BR0#</td><td>I/O</td><td>The BR0# (Bus Request) pin drives the BREQ[0]# signal in the system. During power-up configuration, the central agent asserts the BREQ0# bus signal in the system to assign the symmetric agent ID to the processor. The processor samples it’s BR0# pin on the active-to-inactive transition of RESET# to obtain it’s symmetric agent ID. The processor asserts BR0# to request the system bus.</td></tr>
<tr><td>CPUPRES# (PPGA and FC-PGA only)</td><td>O</td><td>The CPUPRES# signal provides the ability for a system board to detect the presence of a processor. This pin is a ground on the processor indicating to the system that a processor is installed.
The CPUPRES# signal is defined to allow a system design to detect the presence of a terminator device or processor in a PGA370 socket. Combined with the VID combination of VID[3:0]= 1111, a system can determine if a socket is occupied, and whether a processor core is present.
PGA370 Socket Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>0
Anything other than '1111'</td><td>Processor core installed in the PGA370 socket.</td></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>0
1111</td><td>Terminator device installed in the PGA370 socket (i.e., no core present).</td></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>1
Any value</td><td>PGA370 socket not occupied.</td></tr>
</table></td></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the Intel Celeron processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the Intel Celeron processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multicycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.</td></tr>
<tr><td>EDGCTRL</td><td>I</td><td>The EDGCTRL input provides AGTL+ edge control and should be pulled up to VCCCORE with a 51 Ω ± 5% resistor.
NOTE: This signal is NOT used on the FC-PGA package.</td></tr>
<tr><td>EMI
(S.E.P.P. only)</td><td>I</td><td>EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0 Ω) resistors. The zero ohm resistors should be placed in close proximity to the Intel Celeron processor connector. The path to chassis ground should be short in length and have a low impedance. These pins are used for EMI management purposes.</td></tr>
<tr><td>FERR#</td><td>O</td><td>The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.</td></tr>
<tr><td>FLUSH#</td><td>I</td><td>When the FLUSH# input signal is asserted, the processor writes back all data in the Modified state from the internal cache and invalidates all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction.
The processor does not cache any new data while the FLUSH# signal remains asserted.
FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
On the active-to-inactive transition of RESET#, the processor samples FLUSH# to determine its power-on configuration.</td></tr>
<tr><td>HIT#, HITM#</td><td>I/O</td><td>The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all Intel Celeron processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td></tr>
<tr><td>IERR#</td><td>O</td><td>The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Intel Celeron processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic.
The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.</td></tr>
<tr><td>IGNNE#</td><td>I</td><td>The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions.
If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error.
IGNNE# has no effect when the NE bit in control register 0 is set.
IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.</td></tr>
</table>

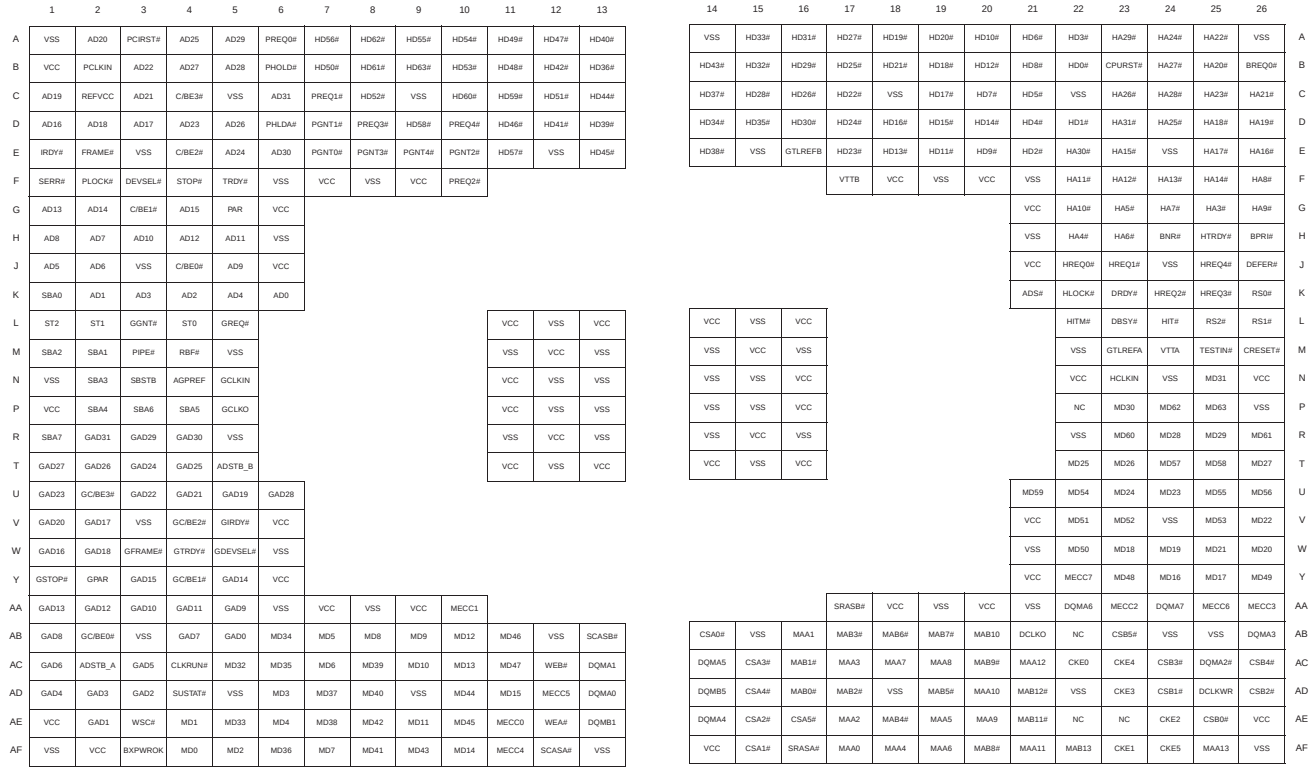
Signal	Type	Description
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of the Intel Celeron processor for proper initialization.
PLL1, PLL2 (PGA packages only)	I	All Intel Celeron processors have internal analog PLL clock generators that require quiet power supplies. PLL1 and PLL2 are inputs to the internal PLL and should be connected to VCCCORE through a low-pass filter that minimizes jitter.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.
PWRGOOD	I	The PWRGOOD (Power Good) signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies (VCCCORE, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state. Figure 39 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 17 and Table 18, and be followed by a 1ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. PWRGOOD Relationship at Power-On 
REQ[4:0]#	I/O	The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 cache without writing back any of the contents. RESET# must stay active for at least one millisecond after VCCCORE and CLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Pentium Pro Family Developerfs Manual, Volume 1: Specifications (Order Number 242690). The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.
RS[2:0]#	I	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RTTCTRL	I	The RTTCTRL input signal provides AGTL+ termination control. The Celeron FC-PGA processor samples this input to sense the presence of motherboard AGTL+ termination.
SLEWCTRL	I	The SLEWCTRL input signal provides AGTL+ slew rate control. The Celeron FC-PGA processor samples this input to determine the slew rate for AGTL+ signals when it is the driving agent.

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>SLOTOCC#
(S.E.P.P. only)</td><td>O</td><td>SLOTOCC# is defined to allow a system design to detect the presence of a terminator card or processor in a SC242 connector. This pin is not a signal; rather, it is a short to VSS. Combined with the VID combination of VID[4:0]= 11111 , a system can determine if a SC242 connector is occupied, and whether a processor core is present. The states and values for determining the type of cartridge in the SC242 connector is shown below.
SC242 Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
Anything other than '1111'</td><td>Processor with core in SC242 connector.</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
1111</td><td>Terminator cartridge in SC242 connector (i.e., no core present).</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>1
Any value</td><td>SC242 connector not occupied.</td></tr>
</table></td></tr>
<tr><td>SLP#</td><td>I</td><td>The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating.
Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.</td></tr>
<tr><td>SMI#</td><td>I</td><td>The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.</td></tr>
<tr><td>STPCLK#</td><td>I</td><td>The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and may latch interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units, resumes execution, and services any pending interrupt. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.</td></tr>
<tr><td>TCK</td><td>I</td><td>The TCK (Test Clock) signal provides the clock input for the Intel Celeron processor Test Access Port.</td></tr>
<tr><td>TDI</td><td>I</td><td>The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.</td></tr>
<tr><td>TDO</td><td>O</td><td>The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.</td></tr>
<tr><td>TESTHI (S.E.P.P. only)</td><td>I</td><td></td></tr>
<tr><td>THERMDN</td><td>O</td><td>Thermal Diode p-n junction. Used to calculate core temperature.</td></tr>
<tr><td>THERMDP</td><td>I</td><td>Thermal Diode p-n junction. Used to calculate core temperature.</td></tr>
<tr><td>THERMTRIP#</td><td>O</td><td>The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135°C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will reassert THERMTRIP# and remain stopped. The system designer should not act upon THERMTRIP# until after the RESET# input is deasserted. Until this time, the THERMTRIP# is indeterminate.</td></tr>
<tr><td>TMS</td><td>I</td><td>The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.</td></tr>
<tr><td>TRDY#</td><td>I</td><td>The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit write-back data transfer. TRDY# must connect the appropriate pins of all system bus agents.</td></tr>
<tr><td>TRST#</td><td>I</td><td>The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Intel Celeron processors require this signal to be driven low during power on Reset. A 680 ohm resistor is the suggested value for a pull down resistor on TRST#.</td></tr>
<tr><td>VCC1.5
(PGA packages only)</td><td>I</td><td>The VCCCMOS pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the VCC2.5 input and 1.5 V must be provided to the VCC1.5 input.
The processor re-routes the 1.5 V input to the VCCCMOS output via the package. The supply for VCC1.5 must be the same one used to supply VTT.</td></tr>
<tr><td>VCC2.5
(PGA packages only)</td><td>I</td><td>The V pin provides the CMOS voltage for use by the platform. The 2.5 V CCCMOS must be provided to the VCC2.5 input and 1.5 V must be provided to the VCC1.5 input.
The processor re-routes the 2.5 V input to the VCCCMOS output via the package.</td></tr>
<tr><td>VCCCMOS
(PGA packages only)</td><td>O</td><td>The VCCCMOS pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the VCC2.5 input and 1.5 V must be provided to the VCC1.5 input.</td></tr>
<tr><td>VCOREDET
(PGA packages only)</td><td>O</td><td>The VCOREDET signal will float for 2.0 V core processors and will be grounded for Celeron FC-PGA processor with a 1.5V core voltage.</td></tr>
<tr><td>VID[4:0]
VID[3:0]
(PGA packages only)</td><td>O</td><td>The VID (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short(S.E.P.P.) circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on Intel Celeron processors.</td></tr>
<tr><td>VREF[7:0]
(PGA packages only)</td><td>I</td><td>These input signals are used by the AGTL+ inputs as a reference voltage. AGTL+inputs are differential receivers and will use this voltage to determine whether the signal is a logic high or logic low.
For the FC-PGA package, VREF is typically 2/3 of VTT</td></tr>
</table>

10. CHIPSET (NORTH BRIDGE)

Intel's 82443BX is used.

10-1. PIN ASSIGHMENTS



	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	AD20	PCIRST#	AD25	AD29	PREQ0#	HD56#	HD62#	HD55#	HD54#	HD49#	HD47#	HD40#
B	VCC	PCLKIN	AD22	AD27	AD28	PHOLD#	HD50#	HD61#	HD63#	HD53#	HD48#	HD42#	HD36#
C	AD19	REFVCC	AD21	C/BE3#	VSS	AD31	PREQ1#	HD52#	VSS	HD60#	HD59#	HD51#	HD44#
D	AD16	AD18	AD17	AD23	AD26	PHLDA#	PGNT1#	PREQ3#	HD58#	PREQ4#	HD46#	HD41#	HD39#
E	IRDY#	FRAME#	VSS	C/BE2#	AD24	AD30	PGNT0#	PGNT3#	PGNT4#	PGNT2#	HD57#	VSS	HD45#
F	SERR#	PLOCK#	DEVSEL#	STOP#	TRDY#	VSS	VCC	VSS	VCC	PREQ2#			
G	AD13	AD14	C/BE1#	AD15	PAR	VCC							
H	AD8	AD7	AD10	AD12	AD11	VSS							
J	AD5	AD6	VSS	C/BE0#	AD9	VCC							
K	SBA0	AD1	AD3	AD2	AD4	AD0							
L	ST2	ST1	GGNT#	ST0	GREQ#						VCC	VSS	VCC
M	SBA2	SBA1	PIPE#	RBF#	VSS						VSS	VCC	VSS
N	VSS	SBA3	SBSTB	AGPREF	GCLKIN						VCC	VSS	VSS
P	VCC	SBA4	SBA6	SBA5	GCLKO						VCC	VSS	VSS
R	SBA7	GAD31	GAD29	GAD30	VSS						VSS	VCC	VSS
T	GAD27	GAD26	GAD24	GAD25	ADSTB_B						VCC	VSS	VCC
U	GAD23	GC/BE3#	GAD22	GAD21	GAD19	GAD28							
V	GAD20	GAD17	VSS	GC/BE2#	GIRDY#	VCC							
W	GAD16	GAD18	GFRAME#	GTRDY#	GDEVSEL#	VSS							
Y	GSTOP#	GPAR	GAD15	GC/BE1#	GAD14	VCC							
AA	GAD13	GAD12	GAD10	GAD11	GAD9	VSS	VCC	VSS	VCC	MECC1			
AB	GAD8	GC/BE0#	VSS	GAD7	GAD0	MD34	MD5	MD8	MD9	MD12	MD46	VSS	SCASB#
AC	GAD6	ADSTB_A	GAD5	CLKRUN#	MD32	MD35	MD6	MD39	MD10	MD13	MD47	WEB#	DQMA1
AD	GAD4	GAD3	GAD2	SUSTAT#	VSS	MD3	MD37	MD40	VSS	MD44	MD15	MECC5	DQMA0
AE	VCC	GAD1	WSC#	MD1	MD33	MD4	MD38	MD42	MD11	MD45	MECC0	WEA#	DQMB1
AF	VSS	VCC	BXPWROK	MD0	MD2	MD36	MD7	MD41	MD43	MD14	MECC4	SCASA#	VSS

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VSS	HD33#	HD31#	HD27#	HD19#	HD20#	HD10#	HD6#	HD3#	HA29#	HA24#	HA22#	VSS
B	HD43#	HD32#	HD29#	HD25#	HD21#	HD18#	HD12#	HD8#	HD0#	CPURST#	HA27#	HA20#	BREQ0#
C	HD37#	HD28#	HD26#	HD22#	VSS	HD17#	HD7#	HD5#	VSS	HA26#	HA28#	HA23#	HA21#
D	HD34#	HD35#	HD30#	HD24#	HD16#	HD15#	HD14#	HD4#	HD1#	HA31#	HA25#	HA18#	HA19#
E	HD38#	VSS	GTLREFB	HD23#	HD13#	HD11#	HD9#	HD2#	HA30#	HA15#	VSS	HA17#	HA16#
F				VTTB	VCC	VSS	VCC	VSS	HA11#	HA12#	HA13#	HA14#	HA8#
G								VCC	HA10#	HA5#	HA7#	HA3#	HA9#
H								VSS	HA4#	HA6#	BNR#	HTRDY#	BPRI#
J								VCC	HREQ0#	HREQ1#	VSS	HREQ4#	DEFER#
K								ADS#	HLOCK#	DRDY#	HREQ2#	HREQ3#	RS0#
L	VCC	VSS	VCC						HITM#	DBSY#	HIT#	RS2#	RS1#
M	VSS	VCC	VSS						VSS	GTLREFA	VTTA	TESTIN#	CRESET#
N	VSS	VSS	VCC						VCC	HCLKIN	VSS	MD31	VCC
P	VSS	VSS	VCC						NC	MD30	MD62	MD63	VSS
R	VSS	VCC	VSS						VSS	MD60	MD28	MD29	MD61
T	VCC	VSS	VCC						MD25	MD26	MD57	MD58	MD27
U								MD59	MD54	MD24	MD23	MD55	MD56
V								VCC	MD51	MD52	VSS	MD53	MD22
W								VSS	MD50	MD18	MD19	MD21	MD20
Y								VCC	MECC7	MD48	MD16	MD17	MD49
AA				SRASB#	VCC	VSS	VCC	VSS	DQMA6	MECC2	DQMA7	MECC6	MECC3
AB	CSA0#	VSS	MAA1	MAB3#	MAB6#	MAB7#	MAB10	DCLKO	NC	CSB5#	VSS	VSS	DQMA3
AC	DQMA5	CSA3#	MAB1#	MAA3	MAA7	MAA8	MAB9#	MAA12	CKE0	CKE4	CSB3#	DQMA2#	CSB4#
AD	DQMB5	CSA4#	MAB0#	MAB2#	VSS	MAB5#	MAA10	MAB12#	VSS	CKE3	CSB1#	DCLKWR	CSB2#
AE	DQMA4	CSA2#	CSA5#	MAA2	MAB4#	MAA5	MAA9	MAB11#	NC	NC	CKE2	CSB0#	VCC
AF	VCC	CSA1#	SRASA#	MAA0	MAA4	MAA6	MAB8#	MAA11	MAB13	CKE1	CKE5	MAA13	VSS

10-2. PIN DISCRIPTION1)HOST INTERFACE SIGNALS

1) Host Interface Signals

■Host Interface Signals

Name	Type	Description
CPURST#	O GTL+	CPU Reset. The CPURST# pin is an output from the 82443BX. The 82443BX generates this signal based on the PCIRST# input (from PIIX4E) and also the SUSTAT# pin in mobile mode. The CPURST# allows the CPUs to begin execution in a known state.
A[31:3]#	I/O GTL+	Address Bus: A[31:3]# connect to the CPU address bus. During CPU cycles, the A[31:3]# are inputs.
HD[63:0]#	I/O GTL+	Host Data: These signals are connected to the CPU data bus. Note that the data signals are inverted on the CPU bus.
ADS#	I/O GTL+	Address Strobe: The CPU bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BNR#	I/O GTL+	Block Next Request: Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O GTL+	Priority Agent Bus Request: The 82443BX is the only Priority Agent on the CPU bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	O GTL+	Symmetric Agent Bus Request: Asserted by the 82443BX when CPURST# is asserted to configure the symmetric bus agents. BREQ0# is negated 2 host clocks after CPURST# is negated.
DBSY#	I/O GTL+	Data Bus Busy: Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O GTL+	Defer: The 82443BX generates a deferred response as defined by the rules of the 82443BXfs dynamic defer policy. The 82443BX also uses the DEFER# signal to indicate a CPU retry response.
DRDY#	I/O GTL+	Data Ready: Asserted for each cycle that data is transferred.
HIT#	I/O GTL+	Hit: Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.

Name	Type	Description
HITM#	I/O GTL+	Hit Modified: Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I GTL+	Host Lock: All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI or AGP snoopable access to DRAM is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O GTL+	Request Command: Asserted during both clocks of request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. The transactions supported by the 82443BX Host Bridge are defined in the Host Interface section of this document.
HTRDY#	I/O GTL+	Host Target Ready: Indicates that the target of the CPU transaction is able to enter the data transfer phase.
RS[2:0]#	I/O GTL+	Response Signals: Indicates type of response according to the following the table: RS[2:0] Response type 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by 82443BX) 100 Hard Failure (not driven by 82443BX) 101 No data response 110 Implicit Writeback 111 Normal data response

Note:

1. All of the signals in the host interface are described in the CPU External Bus Specification. The preceding table highlights 82443BX specific uses of these signals.

■Host Signals Not supported by the 82443BX

Signal	Function	Not Supported By 82443BX
A[35:32]#	Address	Extended addressing (over 4 GB)
AERR#	Address Parity Error	Parity protection on address bus
AP[1:0]#	Address Parity	Parity protection on address bus
BINIT#	Bus Initialization	Checking for bus protocol violation and protocol recovery mechanism
DEP[7:0]#	Data Bus ECC/Parity	Enhanced data bus integrity
IERR#	Internal Error	Direct internal error observation via IERR# pin
INIT#	Soft Reset	Implemented by PIIX4E, BIST supported by external logic.
BERR#	Bus Error	Unrecoverable error without a bus protocol violation
RP#	Request Parity	Parity protection on ADS# and PREQ[4:0]#
RSP#	Response Parity Signal	Parity protection on RS[2:0]#

2) DRAM Interface

■DRAM Interface Signals

Name	Type	Description
RASA[5:0]# /CSA[5:0]# RASB[5:0]# /CSB[5:0]#	O CMOS	Row Address Strobe (EDO): These signals are used to latch the row address on the MAxx lines into the DRAMs. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers. Chip Select (SDRAM): For the memory row configured with SDRAM these pins perform the function of selecting the particular SDRAM components during the active state. Note that there are 2 copies of RAS# per physical memory row to improve the loading.
CKE[3:2] /CSA[7:6]# CKE[5:4] /CSB[7:6]#	O CMOS	Clock Enable: In mobile mode, SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. This CKE function is not supported with Registered DIMMs. Chip Select (SDRAM): These pins perform the function of selecting the particular SDRAM components during the active state. Note that there are 2 copies of CS# per physical memory row to reduce the loading.
CASA[7:0]# /DQMA[7:0]	O CMOS	Column Address Strobe A-side (EDO): The CASA[7:0]# signals are used to latch the column address on the MA[13:0] lines into the DRAMs of the A half of the memory array. These are active low signals that drive the DRAM array directly without external buffering. Input/Output Data Mask A-side (SDRAM): These pins control A half of the memory array and act as synchronized output enables during read cycles and as a byte enables during write cycles.
CASB[1,5]# /DQMB[1,5]	O CMOS	Column Address Strobe B-side (EDO) / Input/Output Data Mask B-side (SDRAM): The same function as a corresponding signals for A side. These signals are used to reduce the loading in an ECC configuration

Name	Type	Description
GCKE/CKE1	O CMOS	Global CKE (SDRAM): Global CKE is used in a 4 DIMM configuration requiring power down mode for the SDRAM. External logic must be used to implement this function. SDRAM Clock Enable (CKE1): In mobile mode, SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. The combination of SDRAMPWR (SDRAM register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register for more details.
SRAS[B,A]#	O CMOS	SDRAM Row Address Strobe (SDRAM): The SRAS[B,A]# signals are multiple copies of the same logical SRASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
CKE0/FENA	O CMOS	SDRAM Clock Enable 0 (CKE0). In mobile mode, CKE0 SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. FET Enable (FENA): In a 4 DIMM configuration. FENA is used to select the proper MD path through the FET switches.
SCAS[B,A]#	O CMOS	SDRAM Column Address Strobe (SDRAM): The SCAS[B,A]# signals are multiple copies of the same logical SCASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
MAA[13:0] MAB[12:11]# MAB[13,10] MAB[9:0]#	O CMOS	Memory Address(EDO/SDRAM): MAA[13:0] and MAB[13:0]# are used to provide the multiplexed row and column address to DRAM. There are two sets of MA signals which drive a max. of 2 DIMMs each. MAA[12:11,9:0] are inverted copies of MAB[12:11,9:0]#. MAA[13,10] and MAB[13,10] are identical copies. Each MAA/MAB[13:0] line has a programmable buffer strength to optimize for different signal loading conditions.
WEA# WEB#	O CMOS	Write Enable Signal (EDO/SDRAM): WE# is asserted during writes to DRAM. The WE# lines have a programmable buffer strength to optimize for different signal loading conditions.
MD [63:0]	I/O CMOS	Memory Data (EDO/SDRAM): These signals are used to interface to the DRAM data bus.
MECC[7:0]	I/O CMOS	Memory ECC Data (EDO/SDRAM): These signals carry Memory ECC data during access to DRAM.

3) PCI Interface (Primary)

■Primary PCI Interface Signals

Name	Type	Description
AD[31:0]	I/O PCI	PCI Address/Data: These signals are connected to the PCI address/data bus. Address is driven by the 82443BX with FRAME# assertion, data is driven or received in the following clocks. When the 82443BX acts as a target on the PCI Bus, the AD[31:0] signals are inputs and contain the address during the first clock of FRAME# assertion and input data (writes) or output data (reads) on subsequent clocks.
DEVSEL#	I/O PCI	Device Select: Device select, when asserted, indicates that a PCI target device has decoded its address as the target of the current access. The 82443BX asserts DEVSEL# based on the DRAM address range or AGP address range being accessed by a PCI initiator. As an input it indicates whether any device on the bus has been selected.
FRAME#	I/O PCI	Frame: FRAME# is an output when the 82443BX acts as an initiator on the PCI Bus. FRAME# is asserted by the 82443BX to indicate the beginning and duration of an access. The 82443BX asserts FRAME# to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an input when the 82443BX acts as a PCI target. As a PCI target, the 82443BX latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which it samples FRAME# active.
IRDY#	I/O PCI	Initiator Ready: IRDY# is an output when 82443BX acts as a PCI initiator and an input when the 82443BX acts as a PCI target. The assertion of IRDY# indicates the current PCI Bus initiator's ability to complete the current data phase of the transaction.
C/BE[3:0]#	I/O PCI	Command/Byte Enable: PCI Bus Command and Byte Enable signals are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. PCI Bus command encoding and types are listed below. C/BE[3:0]# Command Type 0000 Interrupt Acknowledge 0001 Special Cycle 0010 I/O Read 0011 I/O Write 0100 Reserved 0101 Reserved 0110 Memory Read 0111 Memory Write 1000 Reserved 1001 Reserved 1010 Configuration Read 1011 Configuration Write 1100 Memory Read Multiple 1101 Reserved (Dual Address Cycle) 1110 Memory Read Line 1111 Memory Write and Invalidate

Name	Type	Description
PAR	I/O PCI	Parity: PAR is driven by the 82443BX when it acts as a PCI initiator during address and data phases for a write cycle, and during the address phase for a read cycle. PAR is driven by the 82443BX when it acts as a PCI target during each data phase of a PCI memory read cycle. Even parity is generated across AD[31:0] and C/BE[3:0]#.
PLOCK#	I/O PCI	Lock: PLOCK# indicates an exclusive bus operation and may require multiple transactions to complete. When PLOCK# is asserted, non-exclusive transactions may proceed. The 82443BX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
TRDY#	I/O PCI	Target Ready: TRDY# is an input when the 82443BX acts as a PCI initiator and an output when the 82443BX acts as a PCI target. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction.
SERR#	I/O PCI	System Error: The 82443BX asserts this signal to indicate an error condition. The SERR# assertion by the 82443BX is enabled globally via SERRE bit of the PCICMD register. SERR# is asserted under the following conditions: In an ECC configuration, the 82443BX asserts SERR#, for single bit (correctable) ECC errors or multiple bit (non-correctable) ECC errors if SERR# signaling is enabled via the ERRCMD control register. Any ECC errors received during initialization should be ignored. • The 82443BX asserts SERR# for one clock when it detects a target abort during 82443BX initiated PCI cycle. • The 82443BX can also assert SERR# when a PCI parity error occurs during the address or data phase. • The 82443BX can assert SERR# when it detects a PCI address or data parity error on AGP. • The 82443BX can assert SERR# upon detection of access to an invalid entry in the Graphics Aperture Translation Table. • The 82443BX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture and outside of main DRAM range (i.e. in the 640k - 1M range or above TOM). • The 82443BX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture. • The 82443BX asserts SERR# for one clock when it detects a target abort during 82443BX initiated AGP cycle.
STOP#	I/O PCI	Stop: STOP# is an input when the 82443BX acts as a PCI initiator and an output when the 82443BX acts as a PCI target. STOP# is used for disconnect, retry, and abort sequences on the PCI Bus.

Note:

1. All PCI interface signals conform to the PCI Rev 2.1 specification.

4) Primary PCI Sideband Interface

■Primary PCI Sideband Interface Signals

Name	Type	Description
PHOLD#	I PCI	PCI Hold: This signal comes from the PIIX4E. It is the PIIX4E request for PCI bus ownership. The 82443BX will flush and disable the CPU-to-PCI write buffers before granting the PIIX4E the PCI bus via PHLDA#. This prevents bus deadlock between PCI and ISA.
PHLDA#	O PCI	PCI Hold Acknowledge: This signal is driven by the 82443BX to grant PCI bus ownership to the PIIX4E after CPU-PCI post buffers have been flushed and disabled.
WSC#	O CMOS	Write Snoop Complete. This signal is asserted active to indicate that all that the snoop activity on the CPU bus on the behalf of the last PCI-DRAM write transaction is complete and that is safe to send the APIC interrupt message.
PREQ[4:0]#	I PCI	PCI Bus Request: PREQ[4:0]# are the PCI bus request signals used as inputs by the internal PCI arbiter.
PGNT[4:0]#	O PCI	PCI Grant: PGNT[4:0]# are the PCI bus grant output signals generated by the internal PCI arbiter.

5) AGP Interface Signals

There are 17 new signals added to the normal PCI group of signals that together constitute the AGP interface.

The sections below describe their operation and use, and are organized in five groups:

- AGP Addressing Signals
- AGP Flow Control Signals
- AGP Status Signals
- AGP Clocking Signals- Strobes
- PCI Signals

■**AGP Interface Signals**

Name	Type	Description
AGP Sideband Addressing Signals[1]		
PIPE#	I AGP	Pipelined Read: This signal is asserted by the current master to indicate a full width address is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted. When PIPE# is deasserted no new requests are queued across the AD bus. PIPE# is a sustained tri-state signal from masters (graphics controller) and is an input to the 82443BX. Note that initial AGP designs may not use PIPE#.
SBA[7:0]	I AGP	Sideband Address: This bus provides an additional bus to pass address and command to the 82443BX from the AGP master. Note that, when sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).
AGP Flow Control Signals		
RBF#	I AGP	Read Buffer Full. This signal indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted the 82443BX is not allowed to return low priority read data to the AGP master on the first block. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal.
AGP Status Signals		
ST[2:0]	O AGP	Status Bus: This bus provides information from the arbiter to a AGP Master on what it may do. ST[2:0] only have meaning to the master when its GGNT# is asserted. When GGNT# is deasserted these signals have no meaning and must be ignored. 000 Indicates that previously requested low priority read data is being returned to the master. 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously queued write command. 011 Indicates that the master is to provide high priority write data for a previously queued write command. 100 Reserved 101 Reserved 110 Reserved 111 Indicates that the master has been given permission to start a bus transaction. The master may queue AGP requests by asserting PIPE# or start a PCI transaction by asserting FRAME#. ST[2:0] are always an output from the 82443BX and an input to the master.
AGP Clocking Signals - Strobes		
ADSTB_A	I/O AGP	AD Bus Strobe A: This signal provides timing for double clocked data on the AD bus. The agent that is providing data drives this signal. This signal requires an 8.2K ohm external pull-up resistor.
ADSTB_B	I/O AGP	AD Bus Strobe B: This signal is an additional copy of the AD_STBA signal. This signal requires an 8.2K ohm external pull-up resistor.
SBSTB	I AGP	Sideband Strobe: THis signal provides timing for a side-band bus. This signal requires an 8.2K ohm external pull-up resistor.
AGP FRAME# Protocol SIgnals (similar to PCI)[2]		
GFRAME#	I/O AGP	Graphics Frame: Same as PCI. Not used by AGP. GFRAME# remains deasserted by its own pull up resistor.
GIRDY#	I/O AGP	Graphics Initiator Ready: New meaning. GIRDY# indicates the AGP compliant master is ready to provide all write data for the current transaction. Once IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The assertion of IRDY# for reads indicates that the master is ready to transfer to a subsequent block (32 bytes) of read data. The master is never allowed to insert wait states during the initial data transfer (32 bytes) of a read transaction. However, it may insert wait states after each 32 byte block is transferred. (There is no GFRAME# -- GIRDY# relationship for AGP transactions.)
GTRDY#	I/O AGP	Graphics Target Ready: New meaning. GTRDY# indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on both read and write transactions.
GSTOP#	I/O AGP	Graphics Stop: Same as PCI. Not used by AGP.
GDEVSEL#	I/O AGP	Graphics Device Select: Same as PCI. Not used by AGP.
GREQ#	I AGP	Graphics Request: Same as PCI. (Used to request access to the bus to initiate a PCI or AGP request.)
GGNT#	O AGP	Graphics Grant: Same meaning as PCI but additional information is provided on ST[2:0]. The additional information indicates that the selected master is the recipient of previously requested read data (high or normal priority), it is to provide write data (high or normal priority), for a previously queued write command or has been given permission to start a bus transaction (AGP or PCI).
GAD[31:0]	I/O AGP	Graphics Address/Data: Same as PCI.
GC/BE[3:0]#	I/O AGP	Graphics Command/Byte Enables: Slightly different meaning. Provides command information (different commands than PCI) when requests are being queued when using PIPE#. Provide valid byte information during AGP write transactions and are not used during the return of read data.
GPAR	I/O AGP	Graphics Parity: Same as PCI. Not used on AGP transactions, but used during PCI transactions as defined by the PCI specification.

Note:

1. AGP Sideband Addressing Signals. The above table contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. When PIPE# is used to queue addresses the master is not allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism but rather a static decision when the device is first being configured after reset.
2. PCI signals are redefined when used in AGP transactions carried using AGP protocol extension. For transactions on the AGP interface carried using PCI protocol these signals completely preserve PCI semantics. The exact role of all PCI signals during AGP transactions is in Table 2-6.
3. The LOCK# signal is not supported on the AGP interface (even for PCI operations).
4. PCI signals described in Table 2-4 behave according to PCI 2.1 specifications when used to perform PCI transactions on the AGP Interface.

6) Clocks, Reset, and Miscellaneous

■Clocks, Reset, and Miscellaneous

Name	Type	Description
HCLKIN	I CMOS	Host Clock In: This pin receives a buffered host clock. This clock is used by all of the 82443BX logic that is in the Host clock domain. When SUSTAT# is active, there is an internal 100K ohm pull down on this signal.
PCLKIN	I CMOS	PCI Clock In: This is a buffered PCI clock reference that is synchronously derived by an external clock synthesizer component from the host clock. This clock is used by all of the 82443BX logic that is in the PCI clock domain. When SUSTAT# is active, there is an internal 100K ohm pull down on this signal.
DCLKO	O CMOS	SDRAM Clock Out: 66 or 100 MHz SDRAM clock reference. It feeds an external buffer clock device that produces multiple copies for the DIMMs.
DCLKWR	I CMOS	SDRAM Write Clock: Feedback reference from the external SDRAM clock buffer. This clock is used by the 82443BX when writing data to the SDRAM array.
PCIRST#	I CMOS	PCI Reset: When asserted, this signal will reset the 82443BX logic. All PCI output and bi-directional signals will also tri-state compliant to PCI Rev 2.0 and 2.1 specifications. When SUSTAT# is active, there is an internal 100K ohm pull down on this signal.
GCLKIN	I CMOS	AGP Clock In: The GCLKIN input is a feedback reference from the GCLKOUT signal.
GCLKO	O CMOS	AGP Clock Out: The frequency is 66 MHz. The GCLKOUT output is used to feed both the reference input pin on the 82443BX and the AGP compliant device.
CRESET#	O CMOS	Delayed CPU Reset: CRESET# is a delayed copy of CPURST#. This signal is used to control the multiplexer for the CPU strap signals. CRESET# is delayed from CPURST# by two host clocks. Note: This pin requires an external pull-up resistor. If not used, no pull up is required.
TESTIN#	I CMOS	Test Input: This pin is used for manufacturing, and board level test purposes. Note: This pin has an internal 50K ohm pull-up.

■ Power Management Interface

Name	Type	Description
CLKRUN#	I/OD CMOS	Primary PCI Clock Run: The 82443BX requests the central resource (PIIX4E) to start or maintain the PCI clock by the assertion of CLKRUN#. The 82443BX tristates CLKRUN# upon deassertion of PCIRST# (since CLK is running upon deassertion of reset). If connected to PIIX4E an external 2.7K Ohm pull-up is required for Desktop, Mobile requires (8.2k 10K) pull-up. Otherwise, a 100 Ohm pull down is required.
SUSTAT#	I CMOS	Suspend Status (from PIIX): SUSTAT# signals the system suspend state transition from the PIIX4E. It is used to isolate the suspend voltage well and enter/exit DRAM self-refresh mode. During POS/STR SUSTAT# is active.
BXPWROK	I CMOS	BX Power OK: BXPWROK input must be connected to the PWROK signal that indicates valid power is applied to the 82443BX.

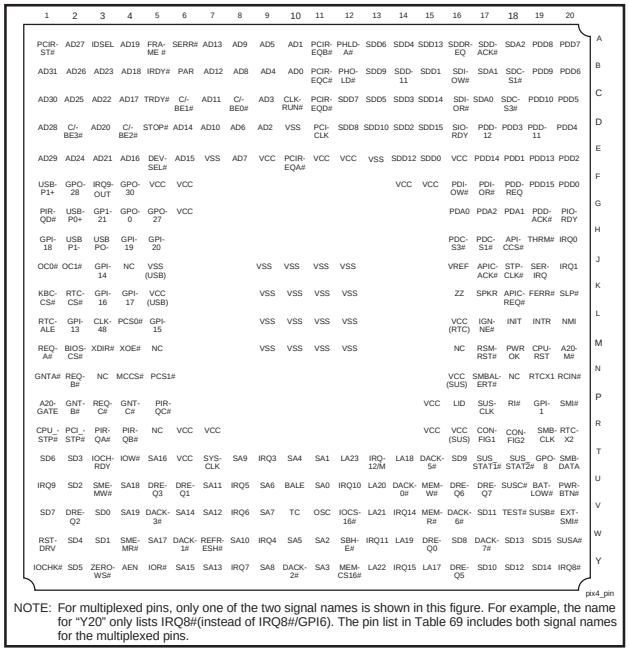
■Reference Pins

Name	Description
GTLREF[B:A]	GTL Buffer voltage reference input
VTT[B:A]	GTL Threshold voltage for early clamps
VCC	Power pin @ 3.3V
VSS	Ground
REF5V	PCI 5V reference voltage (for 5V tolerant buffers)
AGPREF	External Input Reference

11. CHIPSET (SOUTH BRIDGE)

Intel's PIIX4E is used.

11-1. PIN ASSIGHMENTS



NOTE: For multiplexed pins, only one of the two signal names is shown in this figure. For example, the name for "Y20" only lists IRQ8#(instead of IRQ8#/GPI6). The pin list in Table 69 includes both signal names for the multiplexed pins.

11-2. PIN DISCRIPTION

1) PIIX4E Signals

■PCI BUS INTERFACE

Name	Type	Description
AD[31:0]	I/O	PCI ADDRESS/DATA. AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits). During subsequent clocks, AD[31:0] contain data. A PIIX4E Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4E is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4E may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4E drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. During Reset: High-Z After Reset: High-Z During POS: High-Z
C/BE#[3:0]	I/O	BUS COMMAND AND BYTE ENABLES. The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4E drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. During Reset: High-Z After Reset: High-Z During POS: High-Z
CLKRUN#	I/O	CLOCK RUN#. This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described in the PCI Mobile Design Guide, Revision 1.0. During Reset: Low After Reset: Low During POS: High
DEVSEL#	I/O	DEVICE SELECT. PIIX4E asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4E asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4E configuration registers. PIIX4E also asserts DEVSEL# when an internal PIIX4E address is decoded or when PIIX4E subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4E initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4E as a target. During Reset: High-Z After Reset: High-Z During POS: High-Z
FRAME#	I/O	CYCLE FRAME. FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4E when it is the Target. FRAME# is an output when PIIX4E is the initiator. FRAME# remains tri-stated until driven by PIIX4E as an Initiator. During Reset: High-Z After Reset: High-Z During POS: High-Z

Name	Type	Description
IDSEL	I	INITIALIZATION DEVICE SELECT. IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4E samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4E responds by asserting DEVSEL# on the next cycle.
IRDY#	I/O	INITIATOR READY. IRDY# indicates PIIX4Efs ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4E has valid data present on AD[31:0]. During a read, it indicates PIIX4E is prepared to latch data. IRDY# is an input to PIIX4E when PIIX4E is the Target and an output when PIIX4E is an Initiator. IRDY# remains tristated until driven by PIIX4E as a master. During Reset: High-Z After Reset: High-Z During POS: High-Z
PAR	O	CALCULATED PARITY SIGNAL. PAR is gevenh parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. "Even" parity means that the number of "1"s within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4E initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4E is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. During Reset: High-Z After Reset: High-Z During POS: High-Z
PCIRST#	O	PCI RESET. PIIX4E asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4E asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. During Reset: Low After Reset: High During POS: High
PHOLD#	O	PCI HOLD. An active low assertion indicates that PIIX4E desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4E, it may not negate it until PHOLD# is negated by PIIX4E. PIIX4E implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. During Reset: High-Z After Reset: High During POS: High
PHLDA#	I	PCI HOLD ACKNOWLEDGE. An active low assertion indicates that PIIX4E has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	SYSTEM ERROR. SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4E can be programmed to generate a non-maskable interrupt (NMI) to the CPU. During Reset: High-Z After Reset: High-Z During POS: High-Z
STOP#	I/O	STOP. STOP# indicates that PIIX4E, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4E to stop the current transaction. STOP# is an output when PIIX4E is a Target and an input when PIIX4E is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4E as a slave. During Reset: High-Z After Reset: High-Z During POS: High-Z
TRDY#	I/O	TARGET READY. TRDY# indicates PIIX4Efs ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4E, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4E, as a Target is prepared to latch data. TRDY# is an input to PIIX4E when PIIX4E is the Initiator and an output when PIIX4E is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4E as a slave. During Reset: High-Z After Reset: High-Z During POS: High-Z

Note:

All of the signals in the host interface are described in the Pentium Processor data sheet. The preceding table highlights PIIX4E specific uses of these signals.

■ISA BUS INTERFACE

Name	Type	Description
AEN	O	ADDRESS ENABLE. AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4E initiated refresh cycles. During Reset: High-Z After Reset: Low During POS: Low
BALE	O	BUS ADDRESS LATCH ENABLE. BALE is asserted by PIIX4E to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. During Reset: High-Z After Reset: Low During POS: Low
IOCHK#/ GPI0	I	I/O CHANNEL CHECK. IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purpose input.

Name	Type	Description
IOCHRDY	I/O	I/O CHANNEL READY. Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4E owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4E register. As a PIIX4E output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4E latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4E floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4E to float IOCHRDY. PIIX4E does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. During Reset: High-Z After Reset: High-Z During POS: High-Z
IOCS16#	I	16-BIT I/O CHIP SELECT. This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	I/O READ. IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4E owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. During Reset: High-Z After Reset: High During POS: High
IOW#	I/O	I/O WRITE. IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4E owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. During Reset: High-Z After Reset: High During POS: High
LA[23:17]/ GPO[7:1]	I/O	ISA LA[23:17]. LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4E owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. During Reset: High-Z After Reset: Undefined During POS: Last LA/GPO
MEMCS16#	I/O	MEMORY CHIP SELECT 16. MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4E ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4E owns the ISA Bus. PIIX4E drives this signal low during ISA master to PCI memory cycles. During Reset: High-Z After Reset: High-Z During POS: High-Z
MEMR#	I/O	MEMORY READ. MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4E is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4E, owns the ISA Bus. This signal is also driven by PIIX4E during refresh cycles. For DMA cycles, PIIX4E, as a master, asserts MEMR#. During Reset: High-Z After Reset: High During POS: High
MEMW#	I/O	MEMORY WRITE. MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4E owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4E, owns the ISA Bus. For DMA cycles, PIIX4E, as a master, asserts MEMW#. During Reset: High-Z After Reset: High During POS: High
REFRESH#	I/O	REFRESH. As an output, REFRESH# is used by PIIX4E to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4E DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. During Reset: High-Z After Reset: High During POS: High
RSTDRV	O	RESET DRIVE. PIIX4E asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4E asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. During Reset: High After Reset: Low During POS: Low
SA[19:0]	I/O	SYSTEM ADDRESS[19:0]. These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4E owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. During Reset: High-Z After Reset: Undefined During POS: Last SA
SBHE#	I/O	SYSTEM BYTE HIGH ENABLE. SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4E owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. During Reset: High-Z After Reset: Undefined During POS: High
SD[15:0]	I/O	SYSTEM DATA. SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. During Reset: High-Z After Reset: Undefined During POS: High-Z

Name	Type	Description
SMEMR#	O	STANDARD MEMORY READ. PIIX4E asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000h 000FFFFFh) during DMA compatible, PIIX4E master, or ISA master cycles, PIIX4E asserts SMEMR#. SMEMR# is a delayed version of MEMR#. During Reset: High-Z After Reset: High During POS: High
SMEMW#	O	STANDARD MEMORY WRITE. PIIX4E asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1-Mbyte range (00000000h 000FFFFFh) during DMA compatible, PIIX4E master, or ISA master cycles, PIIX4E asserts SMEMW#. SMEMW# is a delayed version of MEMW#. During Reset: High-Z After Reset: High During POS: High
ZEROWS#	I	ZERO WAIT STATES. An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then ZEROWS# is ignored and wait states are added as a function of IOCHRDY.

■X-BUS INTERFACE

Name	Type	Description
A20GATE	I	ADDRESS 20 GATE. This input from the keyboard controller is logically combined with bit 1 (FAST_A20) of the Port 92 Register, which is then output via the A20M# signal.
BIOSCS#	O	BIOS CHIP SELECT. This chip select is driven active during read or write accesses to enabled BIOS memory ranges. BIOSCS# is driven combinatorially from the ISA addresses SA[16:0] and LA[23:17], except during DMA cycles. During DMA cycles, BIOSCS# is not generated. During Reset: High After Reset: High During POS: High
KBCCS#/ GPO26	O	KEYBOARD CONTROLLER CHIP SELECT. KBCCS# is asserted during I/O read or write accesses to KBC locations 60h and 64h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. If the keyboard controller does not require a separate chip select, this signal can be programmed to a general purpose output. During Reset: High After Reset: High During POS: High/GPO
MCCS#	O	MICROCONTROLLER CHIP SELECT. MCCS# is asserted during I/O read or write accesses to IO locations 62h and 66h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. During Reset: High After Reset: High During POS: High
PCS0# PCS1#	O	PROGRAMMABLE CHIP SELECTS. These active low chip selects are asserted for ISA I/O cycles which are generated by PCI masters and which hit the programmable I/O ranges defined in the Power Management section. The X-Bus buffer signals (XOE# and XDIR#) are enabled while the chip select is active. (i.e., it is assumed that the peripheral which is selected via this pin resides on the X-Bus.) During Reset: High After Reset: High During POS: High
RCIN#	I	RESET CPU. This signal from the keyboard controller is used to generate an INIT signal to the CPU.
RTCALE/ GPO25	O	REAL TIME CLOCK ADDRESS LATCH ENABLE. RTCALE is used to latch the appropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes RTCALE to be asserted. RTCALE is asserted on falling IOW# and remains asserted for two SYSCLKs. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. During Reset: Low After Reset: Low During POS: Low/GPO
RTCCS#/ GPO24	O	REAL TIME CLOCK CHIP SELECT. RTCCS# is asserted during read or write I/O accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. During Reset: High After Reset: High During POS: High/GPO
XDIR#/ GPO22	O	X-BUS TRANSCEIVER DIRECTION. XDIR# is tied directly to the direction control of a 74f245 that buffers the X-Bus data, XD[7:0]. XDIR# is asserted (driven low) for all I/O read cycles regardless if the accesses is to a PIIX4E supported device. XDIR# is asserted for memory cycles only if BIOS or APIC space has been decoded. For PCI master initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS or APIC space has been decoded), depending on the cycle type. For ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, PIIX4E negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is driven low from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated high. If the X-Bus is not used, then this signal can be programmed to be a general purpose output. During Reset: High After Reset: High During POS: High/GPO
XOE#/ GPO23	O	X-BUS TRANSCEIVER OUTPUT ENABLE. XOE# is tied directly to the output enable of a 74f245 that buffers the X-Bus data, XD[7:0], from the system data bus, SD[7:0]. XOE# is asserted anytime a PIIX4E supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (BIOSCS#, KBCCS#, RTCCS#, MCCS#) or the Device Resource B (PCCS0#) and Device Resource C (PCCS1#). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI Master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for PCI Master initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus peripheral in which its decode space has been disabled. If an X-Bus not used, then this signal can be programmed to be a general purpose output. During Reset: High After Reset: High During POS: High/GPO

■**DMA SIGNALS**

Name	Type	Description
DACK[0,1,2,3]# DACK[5,6,7]#	O	DMA ACKNOWLEDGE. The DACK# output lines indicate that a request for DMA service has been granted by PIIX4E or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DREQ goes inactive prior to DACK# being asserted, the DACK# signal will not be asserted. During Reset: High After Reset: High During POS: High
DREQ[0,1,2,3] DREQ[5,6,7]	I	DMA REQUEST. The DREQ lines are used to request DMA service from PIIX4Efs DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
REQ[A:C]#/ GPI[2:4]	I	PC/PCI DMA REQUEST. These signals are the DMA requests for PC/PCI protocol. They are used by a PCI agent to request DMA services and follow the PCI Expansion Channel Passing protocol as defined in the PCI DMA section. If the PC/PCI request is not needed, these pins can be used as general-purpose inputs.
GNT[A:C]#/ GPO[9:11]	O	PC/PCI DMA ACKNOWLEDGE. These signals are the DMA grants for PC/PCI protocol. They are used by a PIIX4E to acknowledge DMA services and follow the PCI Expansion Channel Passing protocol as defined in the PCI DMA section. If the PC/PCI request is not needed, these pins can be used as general-purpose outputs. During Reset: High After Reset: High During POS: High/GPO
TC	O	TERMINAL COUNT. PIIX4E asserts TC to DMA slaves as a terminal count indicator. PIIX4E asserts TC after a new address has been output, if the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization. TC is negated before AEN is negated during an autoinitialization. During Reset: Low After Reset: Low During POS: Low

■**INTERRUPT CONTROLLER/APIC SIGNALS**

Name	Type	Description
APICACK#/ GPO12	O	APIC ACKNOWLEDGE. This active low output signal is asserted by PIIX4E after its internal buffers are flushed in response to the APICREQ# signal. When the I/O APIC samples this signal asserted it knows that PIIX4Efs buffers are flushed and that it can proceed to send the APIC interrupt. The APICACK# output is synchronous to PCICLK. If the external APIC is not used, then this is a general-purpose output. During Reset: High After Reset: High During POS: High/GPO
APICCS#/ GPO13	O	APIC CHIP SELECT. This active low output signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. If the external APIC is not used, this pin is a general-purpose output. During Reset: High After Reset: High During POS: High/GPO
APICREQ#/ GPI5	I	APIC REQUEST. This active low input signal is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When PIIX4E samples this pin active it will flush its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, PIIX4E asserts APICACK# which indicates to the external APIC that it can proceed to send the APIC interrupt. The APICREQ# input must be synchronous to PCICLK. If the external APIC is not used, this pin is a general-purpose input.
INTR	OD	INTERRUPT.
IRQ0/ GPO14	O	INTERRUPT REQUEST 0. This output reflects the state of the internal IRQ0 signal from the system timer. If the external APIC is not used, this pin is a general-purpose output. During Reset: Low After Reset: Low During POS: IRQ0/GPO
IRQ1	I	INTERRUPT REQUEST 1. IRQ1 is always edge triggered and can not be modified by software to level sensitive. A low to high transition on IRQ1 is latched by PIIX4E. IRQ1 must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ 3:7, 9:11, 14:15	I	INTERRUPT REQUESTS 3:7, 9:11, 14:15. The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. These interrupts may be programmed for either an edge sensitive or a high level sensitive assertion mode. Edge sensitive is the default configuration. An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ8#/ GPI6	I/O	IRQ 8#. IRQ8# is always an active low edge triggered interrupt and can not be modified by software. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle. If using the internal RTC, then this can be programmed as a general-purpose input. If enabling an APIC, this signal becomes an output and must not be programmed as a general purpose input.
IRQ9OUT#/ GPO29	O	IRQ9OUT#. IRQ9OUT# is used to route the internally generated SCI and SMBus interrupts out of the PIIX4E for connection to an external IO APIC. If APIC is disabled, this signal pin is a General Purpose Output. During Reset: High After Reset: High During POS: IRQ9OUT#/GPO

Name	Type	Description
IRQ 12/M	I	INTERRUPT REQUEST 12. In addition to providing the standard interrupt function as described in the pin description for IRQ[3:7,9:11,14:15], this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt function is selected, a low to high transition on this signal is latched by PIIX4E and an INTR is generated to the CPU as IRQ12. An internal IRQ12 interrupt continues to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected.
PIRQ[A:D]#	I/OD PCI	PROGRAMMABLE INTERRUPT REQUEST. The PIRQx# signals are active low, level sensitive, shareable interrupt inputs. They can be individually steered to ISA interrupts IRQ [3:7,9:12,14:15]. The USB controller uses PIRQD# as its output signal.
SERIRQ/ GPI7	I/O	SERIAL INTERRUPT REQUEST. Serial interrupt input decoder, typically used in conjunction with the Distributed DMA protocol. If not using serial interrupts, this pin can be used as a general-purpose input.

■CPU INTERFACE SIGNALS

Name	Type	Description
A20M#	OD	ADDRESS 20 MASK. PIIX4E asserts A20M# to the CPU based on combination of Port 92 Register, bit 1 (FAST_A20), and A20GATE input signal. During Reset: High-Z After Reset: High-Z During POS: High-Z
CPURST	OD	CPU RESET. PIIX4E asserts CPURST to reset the CPU. PIIX4E asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven inactive a minimum of 2 ms after PWROK is driven active. CPURST is driven active for a minimum of 2 ms when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, PIIX4E resets its internal registers (in both core and suspend wells) to their default state. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. For values During Reset, After Reset, and During POS, see the Suspend/Resume and Resume Control Signaling section.
FERR#	I	NUMERIC COPROCESSOR ERROR. This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4E generates an internal IRQ13 to its interrupt controller unit. PIIX4E then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
IGNNE#	OD	IGNORE NUMERIC EXCEPTION. This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4E coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. During Reset: High-Z After Reset: High-Z During POS: High-Z
INIT	OD	INITIALIZATION. INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4E initiates a soft reset by asserting INIT. PIIX4E also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. Pentium Processor: During Reset: Low After Reset: Low During POS: Low Pentium II Processor: During Reset: High After Reset: High During POS: High
INTR	OD	CPU INTERRUPT. INTR is driven by PIIX4E to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. During Reset: Low After Reset: Low During POS: Low
NMI	OD	NON-MASKABLE INTERRUPT. NMI is used to force a nonmaskable interrupt to the CPU. PIIX4E generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. During Reset: Low After Reset: Low During POS: Low
SLP#	OD	SLEEP. This signal is output to the Pentium II processor in order to put it into Sleep state. For Pentium processor it is a No Connect. During Reset: High-Z After Reset: High-Z During POS: High-Z

Name	Type	Description
SMI#	OD	SYSTEM MANAGEMENT INTERRUPT. SMI# is an active low synchronous output that is asserted by PIIX4E in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. During Reset: High-Z After Reset: High-Z During POS: High-Z
STPCLK#	OD	STOP CLOCK. STPCLK# is an active low synchronous output that is asserted by PIIX4E in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. During Reset: High-Z After Reset: High-Z During POS: High-Z

■CLOCKING SIGNALS

Name	Type	Description
CLK48	I	48-MHZ CLOCK. 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
PCICLK	I	FREE-RUNNING PCI CLOCK. A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4E run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
OSC	I	14.31818-MHZ CLOCK. Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.
RTCX1, RTCX2	I/O	RTC CRYSTAL INPUTS: These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.
SUSCLK	O	SUSPEND CLOCK. 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the Suspend/Resume and Resume Control Signaling section.
SYSCLK	O	ISA SYSTEM CLOCK. SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. During Reset: Running After Reset: Running During POS: Low

■IDE SIGNALS

Name	Type	Description
PDA[2:0]	O	PRIMARY DISK ADDRESS[2:0]. These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector. During Reset: High-Z After Reset: Undefined[1] During POS: PDA
PDCS1#	O	PRIMARY DISK CHIP SELECT FOR 1F0H-1F7H RANGE. For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. During Reset: High After Reset: High During POS: High
PDCS3#	O	PRIMARY DISK CHIP SELECT FOR 3F0-3F7 RANGE. For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. During Reset: High After Reset: High During POS: High
PDD[15:0]	I/O	PRIMARY DISK DATA[15:0]. These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. During Reset: High-Z After Reset: Undefined[1] During POS: PDD
PDDACK#	O	PRIMARY DMA ACKNOWLEDGE. This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4E to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. During Reset: High After Reset: High During POS: High

Name	Type	Description
PDDREQ	I	PRIMARY DISK DMA REQUEST. This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOR#	O	PRIMARY DISK IO READ. In normal IDE this is the command to the IDE device that it may drive data onto the PDD[15:0] lines. Data is latched by PIIX4E on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4E to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. During Reset: High After Reset: High During POS: High
PDIOW#	O	PRIMARY DISK IO WRITE. In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data is latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. During Reset: High After Reset: High During POS: High-Z
PIORDY	I	PRIMARY IO CHANNEL READY. In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4E latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. This is a Schmitt triggered input.
SDA[2:0]	O	SECONDARY DISK ADDRESS[2:0]. These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. During Reset: High-Z After Reset: Undefined[1] During POS: SDA
SDCS1#	O	SECONDARY CHIP SELECT FOR 170H-177H RANGE. For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. During Reset: High After Reset: High During POS: High
SDCS3#	O	SECONDARY CHIP SELECT FOR 370H-377H RANGE. For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. During Reset: High After Reset: High During POS: High-Z
SDD[15:0]	I/O	SECONDARY DISK DATA[15:0]. These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. During Reset: High-Z After Reset: Undefined[1] During POS: SDD

Name	Type	Description
SDDACK#	O	SECONDARY DMA ACKNOWLEDGE. This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4E to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. During Reset: High After Reset: High During POS: High
SDDREQ	I	SECONDARY DISK DMA REQUEST. This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDIOR#	O	SECONDARY DISK IO READ. In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD[15:0] lines. Data is latched by the PIIX4E on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4E to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. During Reset: High After Reset: High During POS: High
SDIOW#	O	SECONDARY DISK IO WRITE. In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. During Reset: High After Reset: High During POS: High
SIORDY	I	SECONDARY IO CHANNEL READY. In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4E latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.

Note:

After reset, all undefined signals on the primary channel will default to the same values as the undefined signals on the secondary channel.

■UNIVERSAL SERIAL BUS SIGNALS

Name	Type	Description
OC[1:0]#	I	OVER CURRENT DETECT. These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0	I/O	SERIAL BUS PORT 0. This signal pair comprises the differential data signal for USB port 0. During Reset: High-Z After Reset: High-Z During POS: High-Z
USBP1+, USBP1	I/O	SERIAL BUS PORT 1. This signal pair comprises the differential data signal for USB port 1. During Reset: High-Z After Reset: High-Z During POS: High-Z

■POWER MANAGEMENT SIGNALS

Name	Type	Description
BATLOW#/ GPI9	I	BATTERY LOW. Indicates that battery power is low. PIIX4E can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general- purpose input.
CPU_STP#/ GPO17	O	CPU CLOCK STOP. Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used as a general-purpose output. For values During Reset, After Reset, and During POS, see the Suspend/Resume and Resume Control Signaling section.
EXTSMI#	I/OD	EXTERNAL SYSTEM MANAGEMENT INTERRUPT. EXTSMI# is a falling edge triggered input to PIIX4E indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4E. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4E in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.
LID/ GPI10	I	LID INPUT. This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a generalpurpose input.
PCIREQ[A:D]#	I	PCI REQUEST. Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/ GPO18	O	PCI CLOCK STOP. Active low control signal to the clock generator used to disable the PCI clock outputs. The PIIX4E free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values During Reset, After Reset, and During POS, see the Suspend/Resume and Resume Control Signaling section.
PWRBTN#	I	POWER BUTTON. Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	RING INDICATE. Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.
RSMRST#	I	RESUME RESET. This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/ GPI11	I	SM BUS ALERT. Input used by System Management Bus logic to generate an interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	SM BUS CLOCK. System Management Bus Clock used to synchronize transfer of data on SMBus. During Reset: High-Z After Reset: High-Z During POS: High-Z
SMBDATA	I/O	SM BUS DATA. Serial data line used to transfer data on SMBus. During Reset: High-Z After Reset: High-Z During POS: High-Z
SUSA#	O	SUSPEND PLANE A CONTROL. Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. During Reset: Low After Reset: High During POS: Low
SUSB#/ GPO15	O	SUSPEND PLANE B CONTROL. Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. During Reset: Low After Reset: High During POS: High/GPO
SUSC#/ GPO16	O	SUSPEND PLANE C CONTROL. Control signal asserted during power management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. During Reset: Low After Reset: High During POS: High/GPO
SUS_STAT1#/ GPO20	O	SUSPEND STATUS 1. This signal is typically connected to the Host-to-PCI bridge and is used to provide information on host clock status. SUS_STAST1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. During Reset: Low After Reset: High During POS: Low/GPO
SUS_STAT2#/ GPO21	O	SUSPEND STATUS 2. This signal will typically connect to other system peripherals and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. During Reset: Low After Reset: High During POS: Low/GPO
THRM#/ GPI8	I	THERMAL DETECT. Active low signal generated by external hardware to start the Hardware Clock Throttling mode. If enabled, the external hardware can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4E to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.
ZZ/ GPO19	O	LOW-POWER MODE FOR L2 CACHE SRAM. This signal is used to power down a cachefs data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. During Reset: Low After Reset: Low During POS: Low

■GENERAL PURPOSE INPUT AND OUTPUT SIGNALS

Some of the General Purpose Input and Output signals are multiplexed with other PIIX4E signals. The usage is determined by thesystem configuration.
The default pin usage is shown in Table 1 and Table 2. The configuration can be selected via the General Configuration register and X-Bus Chip Select register.

Name	Type	Description
GPI[21:0]	I	GENERAL PURPOSE INPUTS. These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h.
GPO[30:0]	O	GENERAL PURPOSE OUTPUTS. These output signals can be controlled via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+34h. If a GPO pin is not multiplexed with another signal or defaults to GPO, then its state after reset is the reset condition of the GPOREG register. If the GPO defaults to another signal, then it defaults to that signal's state after reset. The GPO pins that default to GPO remain stable after reset. The others may toggle due to system boot or power control sequencing after reset prior to their being programmed as GPOs. The GPO8 signal is driven low upon removal of power from the PIIX4E core power plane. All other GPO signals are invalid (buffers powered off).

Table1. GPI Signals

Signal Name	Multiplexed With	Default	Control Register and Bit (PCI Function 1)	Notes
GPI0	IOCHK#	GPI	GENCFG Bit 0	Available as GPI only if in EIO bus mode.
GPI1#		GPI		Non-multiplexed GPI which is always available. This signal when used by power management logic is active low.
GPI[2:4]	REQ[A:C]#	GPI	GENCFG Bits 8 10	Not available as GPI if used for PC/PCI. Can be individually enabled, so for instance, GPI[4] is available if REQ[C]# is not used.
GPI5	APICREQ#	GPI	XBCS Bit 8	Not available as GPI if using an external APIC.
GPI6	IRQ8#	GPI	GENCFG Bit 14	Not available as GPI if using external RTC or external APIC.
GPI7	SERIRQ	GPI	GENCFG Bit 16	Not available as GPI if using Serial IRQ protocol.
GPI8	THRM#	THRM#	GENCFG Bit 23	Not available as GPI if using thermal monitoring.
GPI9	BATLOW#	BATLOW#	GENCFG Bit 24	Not available as GPI if using battery low feature.
GPI10	LID#	LID	GENCFG Bit 25	Not available as GPI if using LID feature.
GPI11	SMBALERT#	SMBALERT#	GENCFG Bit 15	Not available as GPI if using SMBALERT feature
GPI12	RI#	RI#	GENCFG Bit 27	Not available if using ring indicator feature
GPI[13:21]		GPI		Non-multiplexed GPIs which are always available.

Table2. GPO Signals

Signal Name	Multiplexed With	Default	Control Register and Bit (PCI Function 1)	Notes
GPO0		GPO		Non-multiplexed GPO which is always available.
GPO[1:7]	LA[17:23]	GPO	GENCFG Bit 0	Available as GPO only if EIO mode.
GPO8		GPO		Non-multiplexed GPO which is always available. The GPO[8] signal will be driven low upon removal of power from the PIIX4E core power plane.
GPO[9:11]	GNT[A:C]#	GPO	GENCFG Bits [8:10]	Not available as GPO if using for PC/PCI. Can be individually enabled, so GPO[11] is available if REQ[C]# not used.
GPO12	APICACK#	GPO	XBCS Bit 8	Not available as GPO if using external APIC.
GPO13	APICCS#	GPO	XBCS Bit 8	Not available as GPO if using external APIC.
GPO14	IRQ0	GPO	XBCS Bit 8	Not available as GPO if using external APIC.

Signal Name	Multiplexed With	Default	Control Register and Bit (PCI Function 1)	Notes
GPO15	SUSB#	SUSB#	GENCFG Bit 17	Not available as GPO if using for power management.
GPO16	SUSC#	SUSC#	GENCFG Bit 17	Not available as GPO if using for power management.
GPO17	CPU_STP#	CPU_STP#	GENCFG Bit 18	Not available as GPO if using for clock control.
GPO18	PCI_STP#	PCI_STP#	GENCFG Bit 19	Not available as GPO if using for clock control.
GPO19	ZZ	ZZ	GENCFG Bit 20	Not available as GPO if using for power management.
GPO20	SUS_STAT1#	SUS_STAT1#	GENCFG Bit 21	Not available as GPO if using for power management.
GPO21	SUS_STAT2#	SUS_STAT2#	GENCFG Bit 22	Not available as GPO if using for power management.
GPO22	XDIR#	XDIR#	GENCFG Bit 28	Not available as GPO if using X-bus transceiver.
GPO23	XOE#	XOE#	GENCFG Bit 28	Not available as GPO if using X-bus transceiver.
GPO24	RTCCS#	RTCCS#	GENCFG Bit 29	Not available as GPO if using external RTC that doesn't do self decode.
GPO25	RTCALE	RTCALE	GENCFG Bit 30	Not available as GPO if using external RTC that doesn't do self decode.
GPO26	KBCCS#	KBCCS#	GENCFG Bit 31	Not available as GPO if using external KBC that doesn't do self decode.
GPO[27:28]		GPO		Non-multiplexed GPOs which are always available.
GPO29	IRQ9OUT#	GPO	XBCS Bit 8	Not available as GPO if using external APIC. This signal is used for IRQ9 output in APIC mode, where it is level triggered, active low.
GPO30		GPO		Non-multiplexed GPO which is always available.

■OTHER SYSTEM AND TEST SIGNALS

Name	Type	Description
CONFIG1	I	CONFIGURATION SELECT 1. This input signal is used to select the type of microprocessor being used in the system. If CONFIG1=0, the system contains a Pentium microprocessor. If CONFIG1=1, the system contains a Pentium II microprocessor. It is used to control the polarity of INIT and CPURST signals.
CONFIG2	I	CONFIGURATION SELECT 2. This input signal is used to select the positive or subtractive decode of FFFF0000h FFFFFFFFh memory address range (top 64 Kbytes). If CONFIG[2]=0, the PIIX4E will positively decode this range. If CONFIG[2]=1, the PIIX4E will decode this range with subtractive decode timings only. The input value of this pin must be static and may not dynamically change during system operations.
PWROK	I	POWER OK. When asserted, PWROK is an indication to PIIX4E that power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, PIIX4E asserts CPURST, PCIRST# and RSTDRV. When PWROK is driven active (high), PIIX4E negates CPURST, PCIRST#, and RSTDRV.
SPKR	O	SPEAKER. The SPKR signal is the output of counter timer 2 and is internally "ANDed" with Port 061h bit 1 to provide the Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. During Reset: Low After Reset: Low During POS: Last State
TEST#	I	TEST MODE SELECT. The test signal is used to select various test modes of PIIX4E. This signal must be pulled up to VCC(SUS) for normal operation.

■POWER AND GROUND PINS

Name	Type	Description
VCC	V	CORE VOLTAGE SUPPLY. These pins are the primary voltage supply for the PIIX4E core and IO periphery and must be tied to 3.3V.
VCC (RTC)	V	RTC WELL VOLTAGE SUPPLY. This pin is the supply voltage for the RTC logic and must be tied to 3.3V.
VCC (SUS)	V	SUSPEND WELL VOLTAGE SUPPLY. These pins are the primary voltage supply for the PIIX4E suspend logic and IO signals and must be tied to 3.3V.
VCC (USB)	V	USB VOLTAGE SUPPLY. This pin is the supply voltage for the USB input/output buffers and must be tied to 3.3V.
VREF	V	VOLTAGE REFERENCE. This pin is used to provide a 5V reference voltage for 5V safe input buffers. VREF must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, this signal must power up before or simultaneous to VCC. It must power down after or simultaneous to VCC. In a non-5V tolerant system (3.3V only), this signal can be tied directly to VCC. There are then no sequencing requirements.
VSS	V	CORE GROUND. These pins are the primary ground for PIIX4E.
VSS (USB)	V	USB GROUND. This pin is the ground for the USB input/output buffers.

2) Power Planes

PIIX4E has three primary internal power planes. These power planes permit parts of PIIX4E to power down to conserve battery life. Table 3 shows the internal planes and their uses.

Table3. PIIX4E Internal Power Planes

Power Plane	Description	Signals Powered	VCC Pins	GND Pins
RTC	Contains the real-time clock and 256 bytes of battery-backed SRAM. This plane is always powered if the internal RTC is used. If the internal RTC is not used, it may be connected to the suspend plane. Typically, powered via “coin-cell” lithium battery. The input signals attached to the RTC power plane DO NOT SUPPORT 5 VOLT INPUT LEVELS. These signals must not exceed VCC (RTC). There is no reset signal for this power plane.	PWROK, RSMRST#, RTCX1, RTCX2	VCC (RTC)	VSS
SUSPEND	Contains the logic needed to resume from the Suspend-to-Disk and Suspend-to-RAM states. This plane will typically be powered by a power supply which is capable of providing a “trickle” current. The input signals attached to the SUSPEND power plane DO NOT SUPPORT 5 VOLT INPUT LEVELS. These signals must not exceed VCC (SUS). This plane is reset by assertion of the RSMRST# signal.	BATLOW#, CONFIG[1:2], EXTSMI# GPI1, GPO8, IRQ8#, LID, RI# SMBALERT#, SMBCLK SMBDATA, PWRBTN# SUS[A:C]#, SUSCLK SUS_STAT[1:2]#, TEST#	VCC (SUS)	VSS
USB	Contains the USB input/output buffers.	USBP0+, USBP0- USBP1+, USBP1-	VCC (USB)	VSS (USB)
Core	Contains all the rest of the PIIX4E logic. This plane is powered by the main system power supply. All input signals within this plane are 5V tolerant except FERR#. This plane is reset by negation of the PWROK signal.	All Other Signal Pins	VCC	VSS

12. CLOCK GENERATOR

The ICS9248-39 of Integrated Circuit Systems, Inc. is employed as the Clock Generator.

Clock setup is made at Frequency Select Pin (FS0~FS3).

Functionary <Crystal (X1, X2) = 14.31818MHz>

CPU CLOCK	PCI CLOCK(MHz)	FS3	FS2	FS1	FS0
66.8MHz	33.40(CPU/2)	0	0	1	1

13. PS/2 KEYBOARD CONTROLLER

M38813 of Mitsubishi Electric is employed to control the keyboard and the mouse.

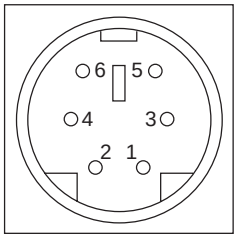
In the UP-5900, IRQ12 is not used and therefore no mouse can be use.

13-1. PIN ASSIGNMENT

No.	Name	Default	Signal	No.	Name	Default	Signal	No.	Name	Default	Signal
33	P17	KSO15	(N.U.)	49	P37	KSI7	(N.U.)	12	P47	KBDDATA	KBDATA
34	P16	KSO14	(N.U.)	50	P36	KSI6	(N.U.)	13	P46	Xkbdclk	KBCLK
35	P15	KSO13	(N.U.)	51	P35	KSI5	(N.U.)	17	P42	AUXDATA	MSDATA
36	P14	KSO12	(N.U.)	52	P34	KSI4	KRTN4	16	P43	xAUXCLK	MSCLK
37	P13	KSO11	(N.U.)	53	P33	KSI3	KRTN3	15	P44	IRQ1	IRQ1
38	P12	KSO10	(N.U.)	54	P32	KSI2	KRTN2	14	P45	IRQ12	(N.U.)
39	P11	KSO9	(N.U.)	55	P31	KSI1	KRTN1	21	P40	xRC	RCIN
40	P10	KSO8	(N.U.)	56	P30	KSI0	KRTN0	20	P41	GATEA20	A20GATE
41	P07	KSO7	(N.U.)	8	P53	HKO7	(P.U.)	25	P27	SCROLL	(N.U.)
42	P06	KSO6	(N.U.)	9	P52	HKO6	(P.U.)	26	P26	NUM	(N.U.)
43	P05	KSO5	KSTB5	10	P51	HKO5	(P.U.)	27	P25	APS	(N.U.)
44	P04	KSO4	KSTB4	11	P50	HKO4	(P.U.)	28	P24	KANA/PAD	(N.U.)
45	P03	KSO3	KSTB3	29	P23	HKO3	(P.U.)	58	P61	TBDATA	(N.U.)
46	P02	KSO2	KSTB2	30	P22	HKO2	(P.U.)	59	P60	TBCLK	(P.U.)
47	P01	KSO1	KSTB1	31	P21	HKO1	(P.U.)				
48	P00	KSO0	KSTB0	32	P20	HKO0	(N.U.)				

13-2. PS2 CONNECTOR PIN ASSIGNMENT

Pin	I/O	Signal
1	I/O	KBDATA
2	I/O	MSDATA
3	-	GND
4	-	+5V
5	I/O	KBCLK
6	I/O	MSCLK
7	-	FG
8	-	FG
9	-	FG



13-3. BUILT-IN KEY PAD

Number of Keys: 27Key (including 10 Key), Max. 30 Keys
(3 of them are 1 × 2Key), Free Key Layout
1 × 2Key has the same Key setup.

Key Layout (Default)

KS05	KS04	KS03	KS02	KS01	KS00	
ESC	F4	F5	F10	Delete	Back Space	← KSI0
7	8	9	Tab	↑	↓	← KSI1
4	5	6	L-Shift	←	→	← KSI2
1	2	3	L-Ctrl	Space		← KSI3
0		00	L-Alt	Enter		← KSI4

14. VIDEO SUB-SYSTEM

Silicon Motion's Graphic Controller (SM722G4) is used to allow control of the LCD Panel (1024 × 768 × RGB TFT). Signals are outputted at LVDS.

14-1. PIN ASSIGNMENTS

Host Interface is of AGP Bus connection. Graphic Memory includes SGRAM of 4Mbyte in 256K × 32-bit × 4 composition.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	MD12	MD3	MD4	MD5	MD7	MD31	MD17	MD28	MD20	MD25	MD22	AD0	AD4	AD7	AD9	AD12	AD14	PAR	~FRAME	~BE2
B	MD2	MD0	MD11	MD9	MD8	~DQM3	MD30	MD18	MD27	MD21	MD24	AD1	AD5	~BE0	AD10	AD13	~BE1	~TRDY	~STOP	AD16
C	MD15	MD1	MD13	MD10	MD6	~DQM2	MD16	MD29	MD19	MD26	MD23	AD3	AD6	AD8	AD11	AD15	~DEVSEL	~IRDY	AD17	AD18
D	~CS0	~DQM1	MD14	VCCA	VSS	MVDD	VSS	MVDD	VSS	VSS	AD2	HVDD	VSS	HVDD	VDD	VSS	HVDD	AD19	AD20	AD21
E	~WE	BA	~DQM0	VSS	RBF#	BA0	RS2	AGP_BUSY#	STOP_AGP#	PIPE#	ST0	ST1	ST2	SBA7	SBA6	SBA5	VSS	AD22	AD23	IDSEL
F	MA5	~CAS	~RAS	MVDD	VCCA											SBA4	HVDD	~BE3	AD24	AD25
G	MA7	MA3	MA4	VSS	VSS											SBA3	VDD	AD26	AD27	AD28
H	MA1	MA8	MA2	MA6	MA10											SBA2	VSS	AD29	AD30	AD31
J	SDCKEN	SDCK	MA9	MA0	VDD											SBA1	HVDD	~REQ	~GNT	CLK
K	VCCA	~ROMEM	DSF	VCCA	PME#											SBA0	VSS	~RST	~INTA	REFCLK
L	MD55	MD56	MD54	VSS	VSS											SB_STB	MCKIN	~PDOWN	~CLKRUN	~EXCKEN
M	MD57	MD53	MD58	VCCA	RS3											VSS	PALCK	VREF	HREF	BLANK
N	MD52	MD59	MD51	VSS	RS4											AD_STB0	P4	P1	P0	PCLK
P	MD60	MD50	MD61	MVDD	VSS											AD_STB1	Y	P5	P3	P2
R	MD49	MD62	MD48	~DQM7	VCCA											LVDD	VPVDD	P8	P7	P6
T	MD63	~DQM6	MD39	VSS	FPVDD	VCCA	VSS	PLLVDD	tx3p	txclkp	txclkn	tx2n	tx1p	tx0p	tx0n	LVSS	C	P12	P10	P9
U	MD40	MD38	MD41	MD43	MVDD	RS12	FDA22	PLLVSS	FPVDD	tx3n	tx2p	FPVDD	tx1n	FPVDDEN	CVSS	AVSS1	USR0	TEST1	P13	P11
V	MD37	MD42	MD34	MD33	~DQM5	FPSCLK	FDA23	FDA19	FDA16	FDA13	FDA8	FDA5	FDA2	VBIASEN	CVDD	RVSS	BLUE	USR1	TEST0	P14
W	MD36	MD46	MD45	MD47	LP	DE	FDA21	FDA18	FDA15	FDA12	FDA9	FDA6	FDA3	FDA0	CRTHSYNC	VDD	IREF	RED	P15	USR2
Y	MD35	MD44	MD32	~DQM4	FP	FPEN	FDA20	FDA17	FDA14	FDA11	FDA10	FDA7	FDA4	FDA1	CRTVSYNC	CKIN	AVDD	GREEN	AVSS2	USR3

PINOUT SM722

VSS	VSS	AVSS3	IREF2
VSS	VSS	VSS	AVDD3
RS5	RS6	RS7	CVBS
RS8	RS9	RS10	RS11

TOP VIEW

14-2. PIN DESCRIPTION

Signal Name	Type	Pull-up/ Pull-Down	Description
Host Interface (PCI or AGP)			
AD [31:0]	I/O		Multiplexed Address and Data Bus. A bus transaction consists of an address cycle followed by one or more data cycles.
C/ ~BE [3:0]	I/O		Bus Command and Byte Enables. These signals carry the bus command during the address cycle and byte enable during data cycles.
PAR	I/O		Parity. Lynx3DM+ asserts this signal to verify even parity across AD [31:0] and C/~BE [3:0].
~FRAME	I/O		Cycle Frame. Lynx3DM+ asserts this signal to indicate the beginning and duration of a bus transaction. It is de-asserted during the final data cycle of a bus transaction.
~TRDY	I/O		Target Ready. A bus data cycle is completed when both ~IRDY and ~TRDY are asserted on the same cycle.
~IRDY	I/O		Initiator Ready. A bus data cycle is completed when both ~IRDY and ~TRDY are asserted on the same cycle.
~STOP	I/O		Stop. Lynx3DM+ asserts this signal to indicate that the current target is requesting the master to stop current transaction.
~DEVSEL	I/O		Device Select. Lynx3DM+ asserts this signal when it decodes its addresses as the target of the current transaction.
IDSEL	I		ID Select. This input is used during PCI configuration read/write cycles.
CLK	I		System Clock, 33MHz. for PCI and 66MHz for AGP
~RST	I		System Reset. Lynx3DM+ asserts this signal to force registers and state machines to initial default values
~REQ	O		Bus Request (bus master mode)
~GNT	I		Bus Grant (bus master mode)
~INTA	O		Interrupt
PME#	O		Power management event signals
~PIPE	O		Pipe signal. Initiates pipelined AGP request. Signal indicates beginning and duration of pipelined AGP access.
~RBF	O		Read Buffer Full. Indicates if graphics device can accept previously low priority read data
AD_STB[1:0]	I/O		Address strobes 1, 0 for 2X transfer support
ST[2:0]	I		Status bus for AGP support
SBA[7:0]	O		Sideband address bits 7-0
SB_STB	O		Sideband strobe
~AGP_BUSY	O		Power management signal for AGP bus.
~STP_AGP	I		Power management signal for AGP bus.
Power Down Interface			

Signal Name	Type	Pull-up/ Pull-Down	Description
~PDOWN	I	pull-up	Power down mode enable
~CLKRUN/ ACTIVITY	O	pull-up	~CLKRUN or Lynx3DM+ Memory and I/O activity detection depending on SCR18 [7] 0 = select ~CLKRUN 1 = select ACTIVITY
Clock Interface			
REFCLK	I	pull-up	32KHz refresh clock source for power down
PALCLK	I	pull-up	27MHz clock source for PAL TV
CKIN	I	pull-up	14.318MHz clock (~EXCKEN = 1) or Video Clock (~EXCKEN = 0)
MCKIN/ LVDSCLK	I/O	pull-up	Memory Clock In (~EXCKEN = 0) LVDSCLK Out (~EXCKEN = 1). LVDSCLK is a free running clock which can be used to drive LVDS transmitter for DSTN panels. Note: this pin is used as CLK2 for dual panel configuration. For this case configure as LVDSCLK.
~EXCKEN	I	pull-up	External Clock Enable. Select external VCLK from CKIN and MCLK from MCKIN.
External Display Memory Interface (for reference only)			
MA [10:0]	O	pull-down	External Memory Address Bus. The video memory row and column addresses are multiplexed on these lines.
MD [63:0]	I/O	MD [63:33] pull-down	
MD [63:0]	I/O	MD[32:0] pull-up	
~WE	O	pull-up	
~RAS	O	pull-up	
~CAS	O	pull-up	External SGRAM Column Address Select
~CS0	O	pull-up	External SGRAM Chip Select 0, select 1st 1MB within the 2MB memory, or select 1st 2MB within the 4MB memory
~DQM [7:0]	O	pull-up	External SGRAM I/O mask [7:0]. DQM [7:0] are byte specific. DQM0 masks MD [7:0], DQM1 masks MD [15:8],Ö,and DQM7 masks MD [63:58].
DSF	O	pull-up	External SGRAM Block write
BA[1:0]	O		External SGRAM Bank Select. SDRAM has 2/4 internal banks. Bank address defines to which bank the current command is being applied.
SDCK	I/O	pull-up	External SGRAM clock. SDCK is driven by the memory clock. All SDRAM input signals are sampled on the positive edge of SDCK.
SDCKEN	I/O	pull-up	External SGRAM clock enable. SDCKEN activates (HIGH) and deactivates (LOW) the SDCLK signal. Deactivating the SDCK provides POWER-DOWN and SELF-REFRESH mode. ~ROMEN
~ROMEN	O	pull-up	ROM Enable

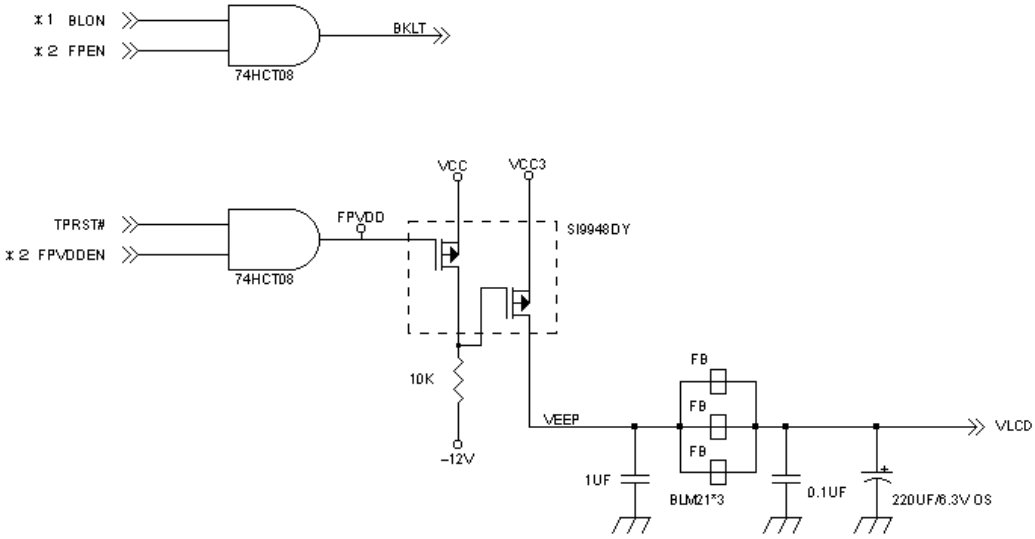
Signal Name	Type	Pull-up/ Pull-Down	Description
Flat Panel Interface			
FDATA [23:0]	O	pull-down	Flat Panel Data Bit 23 to Bit 0 for single panel implementation.
LP/FHSYNC	O	pull-down	**DSTN LCD:** Line Pulse **TFT LCD:** LCD Horizontal Sync
FP/FVSYNC	O	pull-down	DSTN LCD: Frame Pulse TFT LCD: LCD vertical sync
M/DE	O	pull-down	M-signal or Display Enable. This signal is used to indicate the active horizontal display time. FPR3E [7] is used to select 1 = M-signal 0 = Display Enable
FPSCLK	O	pull-down	Flat Panel Shift Clock. This is the pixel clock for Flat Panel Data.
FPEN	O	pull-down	Flat Panel Enable. This signal needs to become active after all panel voltages, clocks, and data are supplied. This signal also needs to become inactive before any panel voltages or control signals are removed. FPEN is part of the VESA FPDI-1B specification.
FPVDDEN	O	pull-down	Flat Panel VDD Enable. This signal is used to control LCD logic power.
VBIASEN	O	pull-down	Flat Panel Voltage Bias Enable. This signal is used to control LCD Bias power.
LVDS Interface			
TX0+/-	O		LVDS Channel 1 Output
TX1+/-	O		LVDS Channel 2 Output
TX2+/-	O		LVDS Channel 3 Output
TX3+/-	O		LVDS Channel 4 Output
TXCLK+/-	O		LVDS Clock Output
CRT Interface			
RED	O		Analog Red Current Output
GREEN	O		Analog Green Current Output
BLUE	O		Analog Blue Current Output
IREF	I		Current Reference Input
CRTVSYNC	O	pull-up	CRT Vertical Sync
CRTHSYNC/ CSYNC	O	pull-up	CRT Horizontal Sync or Composite Sync depending on CCR65 [0] 0 = CRT Horizontal Sync 1 = Composite Sync
TV Interface			
Y	O		Luminance Output
C	O		Chrominance Output
CVBS	O		Composite Video Output
IREF2	I		Current Reference Input
Video Port Interface			

Signal Name	Type	Pull-up/ Pull-Down	Description
P [15:0]	I/O	pull-down	RGB or YUV input/ RGB digital output
PCLK	I/O	pull-up	Pixel Clock
VREF	I/O	pull-up	VSYNC input from PC Card or video decoder
HREF	I/O	pull-up	HSYNC input from PC Card or video decoder
BLANK	O	pull-up	Blank output 0 = BLANK output
General Purpose Registers / I²C			
USR3	I/O	pull-up	General Purpose I/O
USR2	I/O	pull-up	General Purpose I/O
USR1 / SDA	I/O	pull-up	General Purpose I/O. USR1/ DDC2/ I²C Data for CRT. Can be used to select different test modes.
USR0 / SCL	I/O	pull-up	General Purpose I/O. USR0/ DDC2/ I²C Clock for CRT. Can be used to select different test modes.
Test Mode Pins			
TEST [1:0]	I	pull-down	Test mode selects
VCC and GROUND Pins			
HVDD			Host Interface VDD on I/O Ring, 3.3V
MIVDD			Integrated Display Memory Interface VDD on I/O Ring, 3.3V (2.5V option)
MEVDD			External Display Memory Interface VDD on I/O ring, 3.3V (2.5V option)
FPVDD			Flat Panel Interface VDD on I/O Ring, 3.3V
VPVDD			VPort Interface VDD on I/O Ring 3.3V
PLLVDD			LVDS PLL Power Supply, 2.5V
PLLVSS			LVDS PLL Ground
LVDD			LVDS Power Supply, 2.5V
LVSS			LVDS Ground
CVDD			Clock (PLL) Analog Power, 2.5V
AVDD			DAC Analog Power, 3.3V
AVDD3			TVDAC Analog Power, 3.3V
RVDD			RAM Filtered Palette Power, 2.5V
CVSS			PLL Analog Ground
AVSS1			DAC Analog Ground
AVSS2			DAC Analog Ground
AVSS3			TVDAC Analog Ground
RVSS			RAM Filtered Palette Ground
VDD			Digital Core Power Supply, 2.5V
VCCA			Digital Memory Power Supply, 3.3V (2.5V option)

Signal Name	Type	Pull-up/ Pull-Down	Description
VSSA			Digital Internal Memory Ground
VSS			Digital Ground
Others			
RS[12:2]			Reserve pins
BA0			Memory Bank 0 select (Reserved)

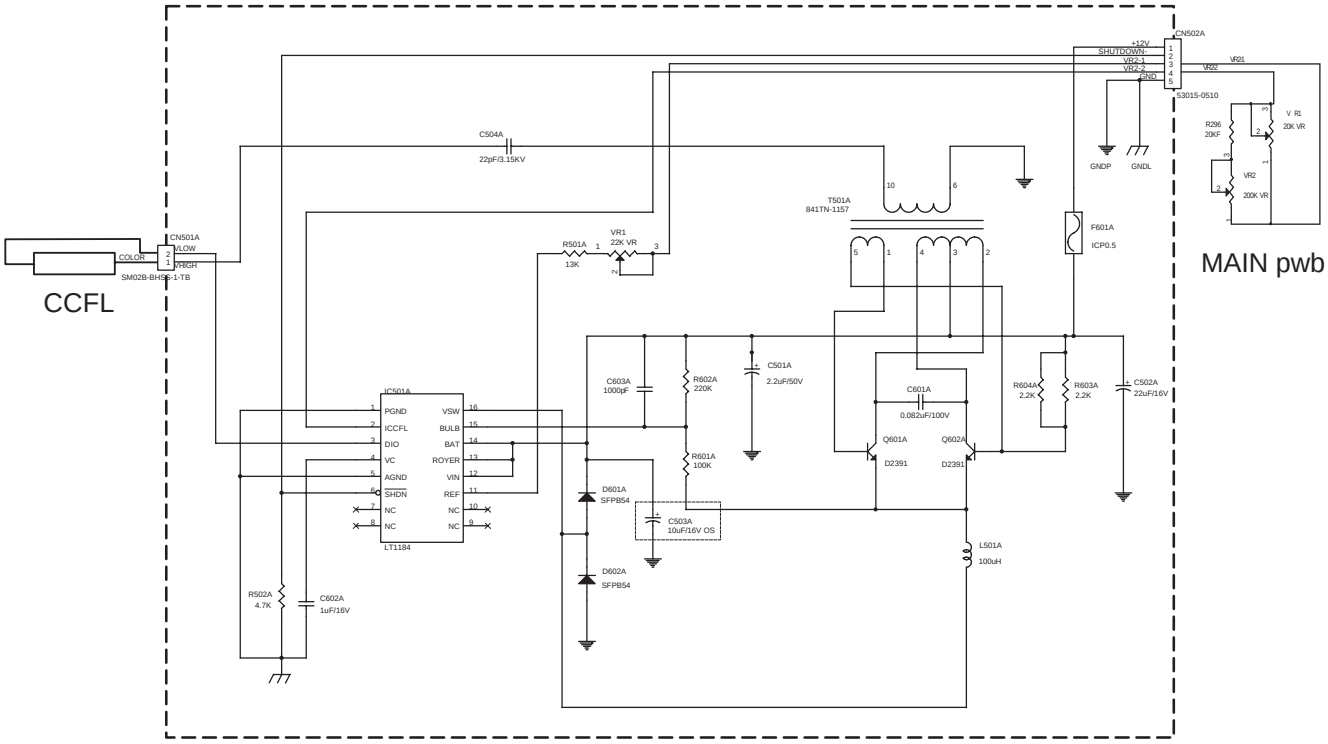
(1) Backlight & LCD power Control

Backlight control and LCD power control can be performed by PSC2 Register control or by SM722G4 control.



*1 : Control signal from PSC2
*2 : Control signal from SM722G4

15. INVERTER CIRCUIT

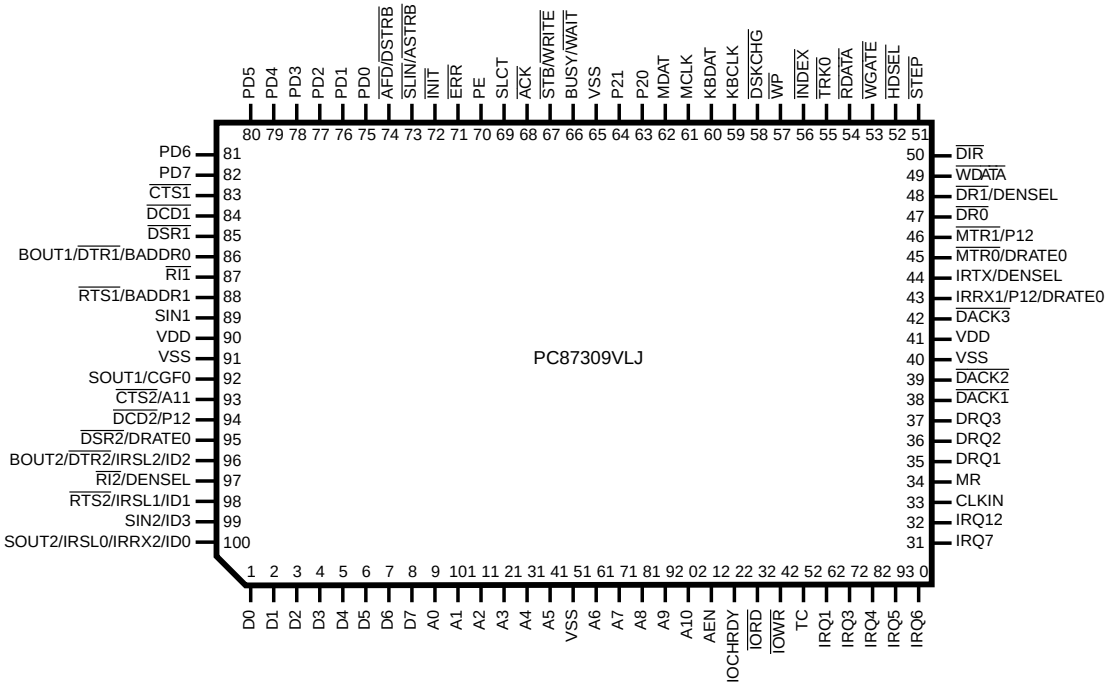


The UP-5900 employs the LT1184 made by Liner Technology for control of brightness (analog control).
The LT1184 detects a current flowing through the low voltage side to vary the switching duty of VSW pin, controlling so that a constant current may flow through the CCFL.
The current flowing through the CCFL can be varied by controlling the current flowing between REF and ICCFL pin of the LT1184.
In the UP-5900, VR1 on the main PWB is operated to change the current flowing between REF and ICCFL pin, controlling the current flowing through the CCFL and adjusting the brightness.

16. ULTRA I/O

National semiconductor's PC87309 is used.

16-1. PIN ASSIGNMENT



16-2. PIN DISCRIPTION

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
A11-0	93, 20-16, 14-9	ISA-Bus	Input Group 1	ISA-Bus Address – A11-0 are used for address decoding on any access except DMA accesses, on the condition that the AEN signal is low. A11 is multiplexed with CTS2 on pin 93 and available in Full-IR mode only. Since A11 is required to support full ISA PnP mode (for decoding A79h), this mode is not available in Two-UART mode.
ACK	68	Parallel Port	Input Group 3	Acknowledge – This input signal is pulsed low by the printer to indicate that it has received data from the parallel port. This pin is internally connected to an internal weak pull-up.
AFD	74	Parallel Port	I/O Group 8	Automatic Feed – When this signal is low the printer should automatically feed a line after printing each line. This pin is in TRISTATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be attached to this pin. This signal is multiplexed with DSTRB.
AEN	21	ISA-Bus	Input Group 1	DMA Address Enable – This input signal disables function selection via A11-0 when it is high. Access during DMA transfer is not affected by this signal. This pin is used for external decoding of A11-15 in Two-UART mode or A15-12 in Full-IR mode.
ASTRB	73	Parallel Port	Output Group 8	Address Strobe (EPP) – This signal is used in EPP mode as an address strobe. It is active low. This signal is multiplexed with SLIN.
BADDR1,0	88,86	Configuration	Input Group 4	Base Address Strap Pins 0 and 1 – These pins determine the base addresses of the Index and Data registers, the value of the Plug and Play ISA Serial Identifier and the configuration state immediately after reset. These pins are pulled down by internal 30 KΩ resistors. External 10 KW pull-up resistors to VDD should be employed. BADDR1 is multiplexed with RTS1. BADDR0 is multiplexed with DTR1 and BOUT1.
BOUT2,1	96,86	UART1, UART2	Output Group 12	Baud Output – This multi-function pin provides the associated serial channel Baud Rate generator output signal if test mode is selected, i.e., bit 7 of the EXCR1 register is set. After Master Reset this pin provides the DTR function. BOUT2 is multiplexed with DTR2, IRSL2 and ID2. BOUT1 is multiplexed with DRT1 and BADDR0.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
BUSY	66	Parallel Port	Input Group 2	Busy – This pin is set high by the printer when it cannot accept another character. It is internally connected to a weak pull-down resistor. This signal is multiplexed with WAIT.
CFG0	92	Configuration	Input Group 4	This pin selects between Full-IR and Two-UART mode as the default configuration upon power up. It is pulled down by internal 30 KΩ resistors. External 10 KW pull-up resistors to VDD should be employed. This signal is multiplexed with SOUT1.
CLKIN	33	Clock	Input Group 1	Clock In – A TTL or CMOS compatible 48 MHz clock.
CTS2,1	93,83	UART1, UART2	Input Group 1	UART1 and UART2 Clear to Send – When low, these signals indicate that the modem or other data transfer device is ready to exchange data. CTS2 is multiplexed with A11, and available only in Two-UART mode.
D7-0	8-1	ISA-Bus	I/O Group 5	ISA-Bus Data – Bidirectional data lines to the microprocessor. D0 is the LSB and D7 is the MSB. These signals have 24 mA (sink) buffered outputs.
DACK3 DACK2,1	42 39,38	ISA-Bus	Input Group 1	DMA Acknowledge 1,2 and 3 – These active low input signals acknowledge a request for DMA services and enable the IOWR and IORD input signals during a DMA transfer. These DMA signals can be mapped to the following logical devices: FDC, UART or Parallel Port.
DCD2,1	94,84	UART1, UART2	Input Group 1	UART1 and UART2 Data Carrier Detected – When low, this signal indicates that the modem or other data transfer device has detected the data carrier. DCD2 is multiplexed with P12 and available only in Two-UART mode.
DENSEL	97, 48 or 44	FDC	Output Group 11	Density Select – Indicates that a high FDC density data rate (500 Kbps or 1 Mbps) or a low density data rate (250 or 300 Kbps) is selected. DENSEL polarity is controlled by bit 5 of the SuperI/O FDC Configuration register as described in Section 2.5.1. This signal is multiplexed with: IRTX, , DR1, or R12.
DIR	50	FDC	Output Group 11	Direction – This output signal determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in, inactive = step out) during a seek operation. During reads or writes, DIR is inactive.
DR1,0	48, 47	FDC	Output Group 11	Drive Select 0 and 1 – These active low output signals are the decoded drive select output signals. DR0 and DR1 are controlled by Digital Output Register (DOR) bits 0 and 1. They are encoded with information to control four FDDs when bit 7 of the SuperI/O FDC Configuration register is 1, as described in Section 2.5.1. DR0 can optionally become a logical OR of DR0 and MTR0 when MTR0/DRATE0 is used as DRATE0. DR1 is multiplexed with DENSEL and is available only in Two-UART mode. Optionally, it can become a logical OR of DR1 and MTR1 when MTR1/P12 is used as P12.
DRATE0	95, 45 or 43	FDC	Output Group 14	Data Rate 0 – This output signal reflects the value of bit 0 of the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last. Output from the pin is totem-pole buffered (6 mA sink, 6 mA source). This signal is multiplexed with IRRX1/P12, MTR0 or DSR2
DRQ3-1	37-35	ISA-Bus	Output Group 13	DMA Request 1, 2 and 3 – These active high output signals inform the DMA controller that a data transfer is needed. These DMA signals can be mapped to the following logical devices: Floppy Disk Controller (FDC), UART or parallel port.
DSKCHG	58	FDC	Input Group 1	Disk Change – This input signal indicates whether or not the drive door has been opened. The state of this pin is available from the Digital Input Register (DIR). This pin can also be configured as the RGATE data separator diagnostic input signal via the MODE command.
DSR2,1	95,85	UART1, UART2	Input Group 1	Data Set Ready – When low, this signal indicates that the data transfer device, e.g., modem, is ready to establish a communications link. DSR2 is multiplexed with DRATE0 and available only in Two-UART mode.
DSTRB	74	Parallel Port	Output Group 8	Data Strobe – This signal is used in EPP mode as a data strobe. It is active low. DSTRB is multiplexed with AFD.
DTR2,1	96,86	UART1, UART2	Output Group 12	Data Terminal Ready – When low, this output signal indicates to the modem or other data transfer device that the UART1 or UART2 is ready to establish a communications link. A Master Reset (MR) deactivates this signal high, and loopback operation holds this signal inactive. DTR1 is multiplexed with BADDR0 and with BOUT1. DTR2 is multiplexed with IRSL2/ID2/BOUT2 and is available only in Two-UART mode. (BOUT2 is multiplexed implicitly and controlled by UART2.)
ERR	71	Parallel Port	Input Group 3	Error – This input signal is set active low by the printer when it has detected an error. This pin is internally connected to an internal weak pull-up.
HDSEL	52	FDC	Output Group 11	Head Select – This output signal determines which side of the FDD is accessed. Active low selects side 1, inactive selects side 0.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
ID3 ID2 ID1 ID0	99 96 98 100	UART2	Input Group 1	Identification – These ID signals identify the infrared transceiver for Plug and Play support. These pins are read after reset. ID0,1,2 are multiplexed implicitly with IRSL0,1,2 respectively by the UART2 cell. ID3 is multiplexed with SIN2. ID2 is multiplexed with BOUT2, $\overline{\text{DTR2}}$, IRSL2. ID1 is multiplexed with $\overline{\text{RTS2}}$, IRSL1 ID0 is multiplexed with SOUT2,IRSL0, IRRX2
$\overline{\text{INDEX}}$	56	FDC	Input Group 1	Index – This input signal indicates the beginning of an FDD track.
$\overline{\text{INIT}}$	72	Parallel Port	I/O Group 8	Initialize – When this signal is active low, it causes the printer to be initialized. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed.
IOCHRDY	22	ISA-Bus	Output Group 15	I/O Channel Ready – This is the I/O channel ready open drain output signal. When IOCHRDY is driven low, the EPP extends the host cycle.
$\overline{\text{IORD}}$	23	ISA-Bus	Input Group 1	I/O Read – An active low $\overline{\text{RD}}$ input signal indicates that the microprocessor has read data.
$\overline{\text{IOWR}}$	24	ISA-Bus	Input Group 1	I/O Write – $\overline{\text{WR}}$ is an active low input signal that indicates a write operation from the microprocessor to the controller.
IRQ1 IRQ7-3 IRQ12	26 31-27 32	ISA-Bus	I/O Group 10	Interrupt Requests 1, 3, 4, 5, 6, 7 and 12 – IRQ polarity and push-pull or open-drain output selection is software configurable by the logical device mapped to the IRQ line. Keyboard Controller (KBC) or Mouse interrupts can be configured by the Interrupt Request Type Select 0 register (index 71h) as either edge or level.
IRRX2,1	100,43	UART2	Input Group 18	Infrared Reception 1 and 2 – Infrared serial input data. IRRX1 is multiplexed with P12/DRATE0 and is available only in Two UART mode. IRRX2 is multiplexed with SOUT2/IRSL0/ID0 and is available only in Full-IR mode.
IRSL0 IRSL1 IRSL2	100 98 96	UART2	Output Group 12	Infrared Control Signals 0, 1 and 2 – These signals control the Infrared analog front end. The pins on which these signals are driven is determined by the SuperI/O Configuration 2 register (index 22h). IRSL0 is multiplexed on pin 100 with SOUT2, IRRX2 and ID0, and is available only in Full-IR mode. IRSL1 is multiplexed on pin 98 with $\overline{\text{RTS2}}$ and ID1, and is available only in Full-IR mode. IRSL2 is multiplexed on pin 96 with $\overline{\text{DTR2}}$, BOUT2 and ID2, and is available only in Full-IR mode.
IRTX	44	UART2	Output Group 12	Infrared Transmit – Infrared serial output data. This signal is multiplexed with DENSEL only in Two-UART mode.
KBCLK	59	KBC	I/O Group 6	Keyboard Clock – This I/O pin transfers the keyboard clock between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is connected internally to the internal TO signal of the KBC.
KBDAT	60	KBC	I/O Group 6	Keyboard Data – This I/O pin transfers the keyboard data between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is connected internally to KBCfs P10.
MCLK	61	KBC	I/O Group 6	Mouse Clock – This I/O pin transfers the mouse clock between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is connected internally to KBCfs T1.
MDAT	62	KBC	I/O Group 6	Mouse Data – This I/O pin transfers the mouse data between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is connected internally to KBCfs P11.
MR	34	ISA-Bus	Input Group 1	Master Reset – An active high MR input signal resets the controller to the idle state, and resets all disk interface output signals to their inactive states. MR also clears the DOR, DSR and CCR registers, and resets the MODE command, CONFIGURE command, and LOCK command parameters to their default values. MR does not affect the SPECIFY command parameters. MR sets the configuration registers to their selected default values.
$\overline{\text{MTR1,0}}$	46,45	FDC	Output Group 11	Motor Select 1,0 – These motor enable lines for drives 0 and 1 are controlled by bits D7-4 of the Digital Output Register (DOR). They are output signals that are active when they are low. They are encoded with information to control four FDDs when bit 7 of the SuperI/O FDC Configuration register is set See $\overline{\text{DR1,0}}$. $\overline{\text{MTR0}}$ is multiplexed with DRATE0 only in Two-UART mode. $\overline{\text{MTR1}}$ is multiplexed with P12 only in Two-UART mode.
P12	94, 46 or 43	KBC	I/O Group 7	I/O Port – KBC quasi-bidirectional port for general purpose input and output. P12 is multiplexed on pin 43 with IRRX1 and DRATE0, on pin 46 with $\overline{\text{MTR1}}$, and on pin 94 with $\overline{\text{DCD2}}$.
P21,P20	64,63	KBC	I/O Group 7	I/O Port – KBC open-drain signals for general purpose input and output. These signals are controlled by KBC firmware.

Signal/Pin Name	Pin Number	Module	I/O and Group #	Function
PD7-0	82-75	Parallel Port	I/O Group 9	Parallel Port Data – These bidirectional signals transfer data to and from the peripheral data bus and the appropriate parallel port data register. These signals have a high current drive capability.
PE	70	Parallel Port	Input Group 2 Group 3	Paper End – This input signal is set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.
$\overline{\text{RDATA}}$	54	FDC	Input Group 1	Read Data – This input signal holds raw serial data read from the Floppy Disk Drive (FDD).
$\overline{\text{RI2,1}}$	97,87	UART1	Input Group 1	Ring Indicators (Modem) – When low, this signal indicates that a telephone ring signal has been received by the modem. The $\overline{\text{RI1}}$ and $\overline{\text{RI2}}$ pins have schmitt-trigger input buffers. $\overline{\text{RI2}}$ is multiplexed with DENSEL and available only in Two-UART mode.
$\overline{\text{RTS2,1}}$	98,88	UART1, UART2	Output Group 12	Request to Send – When low, these output signals indicate to the modem or other data transfer device that the corresponding UART1 or UART2 is ready to exchange data. A Master Reset (MR) sets $\overline{\text{RTS}}$ to inactive high. Loopback operation holds it inactive. $\overline{\text{RTS2}}$ is multiplexed on pin 98 with IRSL1 and ID1, and available only in Two-UART mode. $\overline{\text{RTS1}}$ is multiplexed on pin 88 with BADDR1.
SIN2,1	99,89	UART1, UART2	Input Group 1	Serial Input – This input signal receives composite serial data from the communications link (peripheral device, modem or other data transfer device). SIN2 is multiplexed on pin 99 with ID3 and available only in Two-UART mode.
SLCT	69	Parallel Port	Input Group 2	Select – This input signal is set active high by the printer when the printer is selected. This pin is internally connected to a nominal 25KΩ pull-down resistor.
$\overline{\text{SLIN}}$	73	Parallel Port	I/O Group 8	Select Input – When this signal is active low it selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. Use an external 4.7 KW pull-up resistor. This signal is multiplexed with $\overline{\text{ASTRB}}$.
SOUT2,1	100,92	UART1, UART2	Output Group 12	Serial Output – This output signal sends composite serial data to the communications link (peripheral device, modem or other data transfer device). The SOUT2,1 signals are set active high after a Master Reset (MR). SOUT2 is multiplexed on pin 100 with IRRX2, IRSL0 and ID0, and is available only in Two-UART mode. SOUT1 is multiplexed on pin 92 with CFG0.
STB	67	Parallel Port	I/O Group 8	Data Strobe – This output signal indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed. This signal is multiplexed with $\overline{\text{WRITE}}$.
$\overline{\text{STEP}}$	51	FDC	Output Group 11	Step – This output signal issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
TC	25	ISA-Bus	Input Group 1	DMA Terminal Count – The DMA controller issues TC to indicate the termination of a DMA transfer. TC is accepted only when a $\overline{\text{DACK}}$ signal is active. TC is active high in PC-AT mode, and active low in PS/2 mode.
$\overline{\text{TRK0}}$	55	FDC	Input Group 1	Track 0 – This input signal indicates to the controller that the head of the selected floppy disk drive is at track 0.
VDD	90,41	Power Supply	Input	Main 5 V Power Supply – This signal is the 5 V supply voltage for the digital circuitry.
VSS	91,65,40, 15	Power Supply	Output	Ground – This signal provides the ground for the digital circuitry.
$\overline{\text{WAIT}}$	66	Parallel Port	Input Group 2	Wait – In EPP mode, the parallel port device uses this signal to extend its access cycle. $\overline{\text{WAIT}}$ is active low. This signal is multiplexed with BUSY.
$\overline{\text{WDATA}}$	49	FDC	Output Group 11	Write Data (FDC) – This output signal holds the write precompensated serial data that is written to the selected floppy disk drive. Precompensation is software selectable.
$\overline{\text{WGATE}}$	53	FDC	Output Group 11	Write Gate (FDC) – This output signal enables the write circuitry of the selected disk drive. $\overline{\text{WGATE}}$ is designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.
$\overline{\text{WP}}$	57	FDC	Input Group 1	Write Protected – This input signal indicates that the disk in the selected drive is write protected.
$\overline{\text{WRITE}}$	67	Parallel Port	Output Group 8	Write Strobe – In EPP mode, this active low signal is a write strobe. This signal is multiplexed with $\overline{\text{STB}}$.

17. POS SYSTEM CONTROLLER 2

This is connected to ISA bus by using Sharp's LZ9AM22, and used to control POS devices.

Special System Register 1: 07F1h

SSR1	b7	b6	b5	b4	b3	b2	b1	b0
Read	A9	A8	A7	A6	0	0	SDEN	0
Write	A9	A8	A7	A6	0	0	SDEN	0

bit7: Offset address (A9) default = 0 / UP-5900 = 0

bit6: Offset address (A8) default = 1 / UP-5900 = 1

bit5: Offset address (A7) default = 0 / UP-5900 = 1

bit4: Offset address (A6) default = 0 / UP-5900 = 0

Registers except for SSR0 (07F0h) and SSR1 (07F1h) inside PSC2 can be set to Relocatable in the unit of 40h by the above offset address setup. Therefore the address of a relocatable register is expressed as (PSC2+***h) =@@@h.

bit3: not used

bit2: not used

bit1: Shut Down Enable

SDEN = 0 : Enable (Default)

SDEN = 1 : Disable

bit0: not used

17-1. PSC2 FEATURE OUTLINE

Sharpfs LZ9A10000 is used as the PSC2, controlling the devices

connected to the ISA bus.

BIOS ROM control

MASK ROM control

ROM and RAM disk control

The PSC2 internally expands dedicated interrupts to allow ISA interrupts

to be assigned.

Incorporated DOS convertible UART2 channel

Incorporated UART2 channel for VFD I/F

Incorporated UART1 channel for touch panel

Incorporated 2 channels of MCR I/F

Incorporated 4 channels of drawer I/F

Incorporated 2 channels of CKDC I/F

Incorporated mode key I/F and clerk key I/F

Supported input ports of system SW

Incorporated 2 channels of 8-bit timer counter

Decoded output of super I/O upper address

Reset control

17-2. MEMORY CONTROL (NOT USED)

17-3. I/O CONTROL

(1) Special System Register

The special system register has a input port reading setup data defining the system configuration of hardware and software, offset register setting a base address to relocatably place each internal register of the PSC2 on the I/O space, COM decode control register, and shut-down register.

This special system register uses fixed I/O address ranging from 07F0H to 07F1H. This address is in the area used by the FDC, however this address is non-selected address of super I/O. So sys-tems using the PSC2 are limited to a system in which address 07F0H to 07F1H is not selected as an address decoded by the FDC, or a system which uses the super I/O chip.

(2) Interrupt Expansion and Assign Control

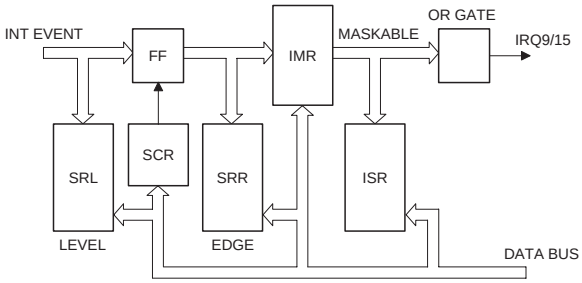
The interrupt control lines on the ISA bus used in the PSC2 are 6 lines: IRQ3, IRQ4, IRQ9, IRQ10, IRQ11, and IRQ15.

Each interrupt control line is outputted by taking OR between signals on the ISA bus and the interrupt signal in the PSC2. UART2 can be assigned to IRQ2, and UART1 can be assigned to IRQ4. PC-X dedicated interrupt (IRQX) can be assigned to IRQ9. UART1, 2, and 5 can be assigned to IRQ10 and 11. UART1/2 and IRQX can be as-signed to IRQ15.

IRQX is a signal generated by taking OR among interrupt control from the POS dedicated device.

Assignment to each IRQ is controlled according to the setting of interrupt assign register 0 and 1 (IAR0 and 1).

The PSC2 internal interrupt expansion consists of a maskable inter-rupt source register (ISR), which is the source of interface OR-com-posed from each interrupt input, interrupt mask register (IMR) control-ling the mask control, status read level register (SRL) reading the status of input which is not masked, status read register (SRR) read-ing edges, and status clear register (SCR) generating edges for the next interrupt.



IBM-PCfs 8259 is programmed based on rising edges and incorporates edge generators on the rear step of each interrupt handling of level input. Edges are generated based on the output of OR-composition when performing dummy writing to the SCR.

The steps generating an edge for general interrupts are as follows:

1) Read the ISR.
2) Check the factor of interrupt.
3) Perform the handling of interrupt for each factor.
4) Write clear the corresponding SCR bit to generate the following edge.
   Read in interrupt disable state and clear the corresponding bit to “1” to write.
5) Return from the interrupt handling.

(3) RS232 Interface

2 UARTs (8250) for RS232 are incorporated in the PSC2 as a Mega Macro Function. UART1 and 2 are decoded as follows by the setting of bit 7 of the SSR0 register.

Bit 7: CMOS (decode control of UART1 and 2)

SW7=1: DOS compatible COM3/COM4 mode (initial value)

COM3: 3E8H to 3EFH (8-byte address)

COM4: 2E8H to 2EFH (8-byte address)

SW7=0: Unique decode mode

Unique: PSC2+410H (16-byte address)

i.e. UART1 unit: PSC2+(410-417H)

UART2 unit: PSC2+(418-41FH)

The assignment of interrupt can be freely defined using system SW6 of special system register 0 and the assign register.

The hardware configuration conforms to the RS232 of AT specifications.

(4) Drawer Interface

The I/O port driving the drawer solenoid is composed of the internal gates of PSC2.

When power off (ACL signal = “0”) is detected, each output port is preset and the driving of the drawer solenoid is immediately stopped.

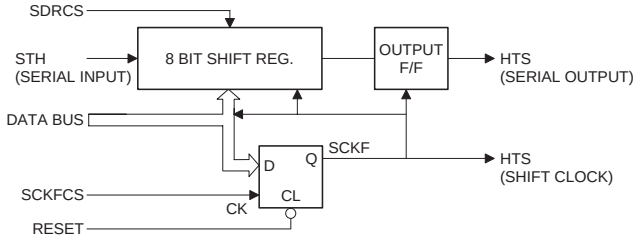
The driving time of the drawer solenoid is automatically set to 45ms by the hardware timer control after turning each drive port ON.

(5) CKDC Interface

As previously defined, the CKDC interface, is 2 sets of 8-bit serial interface is incorporated in the PSC2. This interface is composed of an 8-bit parallel-in/parallel-out shift register and a SCKF register for generating shift clock. Also CKDCRES1/2 signals (reset of CKDC) and SHEN1/2# signals (shift enable signal) must be prepared as CKDC interface. However SHEN1/2# are used in the PSC2 as dedi-cated signal pins inputting interrupt events.

SCKF is outputted to SCK pin without the logic changed and preset to “1” by RESET. The serial data is in the form of LSB first. SCKF operates with synchronized with SCK, and the operation speed depends on the speed of CPU because the shift operation needs to clear and set SCKF by software control for each bit.

STH is shifted in by the rising of SCK, and shifted out by the falling of SCK. The shift-in and shift-out have a margin to the delay of line because of 1/2 bit of phase difference.



(6) Timer Counter

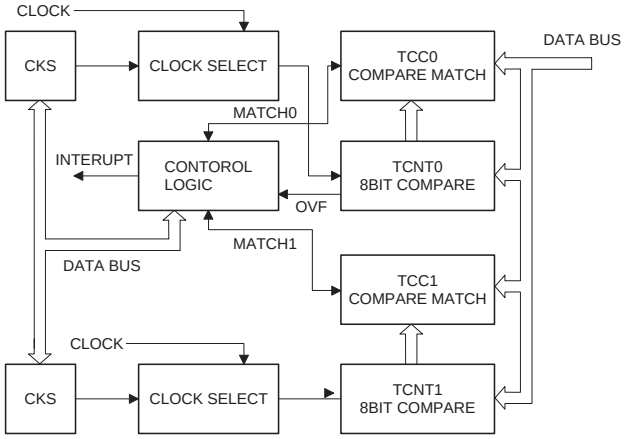
The PSC2 incorporates 2 8-bit hardware free run counters necessary to control dedicated devices. This 8-bit counter can be read or written as TCNT register 0 and 1, counted up by input clock. This input clock is selected using CLOCK SELECT (2 bits respectively) of the TCR register. When TCNT0 is equal to the value of timer compare con-stant register (TCC0), compare match signal can be generated and a maskable interrupt can be generated. Also when TCNT1 is equal to TCC1, compare match signal can be generated and a maskable interrupt can be generated. When the TCNT0 overflows, an overflow signal can be generated and a maskable interrupt can be generated.

Types of internal timer interrupt

IS14: TINT0# (timer compare match interrupt 0)

IS13: TINT1# (timer compare match interrupt 1)

IS12: TOINT# (timer overflow interrupt)



(7) MCR Interface

This interface has 2 channels containing 96 bytes of FIFO respective-ly.

Read data are stored in the FIFO. Each channel functions inde-pendently, so the 2 channels can be read simultaneously.

Description of Read Operation

1) The MCR interface goes into the status of waiting for reading a card after the following settings are performed by the main CPU.
   - Setting a mode: Sets a mode corresponding to the standard of the handled card (JBA/ABA/IATA).
   - Setting a start mark: Sets a start mark corresponding to the standard of the card.
   - Resetting the interrupt: Resets the interrupt because no card can be read when any interrupt is active.
2) After a card is scanned, the MCR interface changes serial data of the MCR to parallel data. Changed data is written in the FIFO buffer at every character in order from the start mark to the LRC.
   The FIFO buffer has the capacity of 96 bytes, and the number of characters in a card corresponding to each standard is as follows:

   JBA (JIS II type): 72 characters maximum (8 bits a character)

   ABA (MEGA MACRO FUNCTION II type second track): 40 characters maximum (5 bits a character)

   IATA (JIS I type first track): 79 characters maximum (7 bits a character)

   The 2 FIFOs are prepared independently to 2 channels of interface.
   These FIFOs can be read simultaneously when connected to a MCR corresponding to JBA/ABA or IATA/ABA.

3) When a card has been scanned, interrupts for the MCR interface are activated.

4) The main CPU reads taken card data from the FIFO buffer in the interrupt handling. The main CPU can read the data using IN command of 0WAIT.
   Even after the LCR which is the last character of a card was read, 10 to 20 characters of “0” remains in the FIFO buffers. So it is necessary to reset the FIFO before read enabling the next card after reading the LCR of the last data.

5) This MCR interface does not read the next card until interrupts are reset by the main CPU.

(8) VFD Interface

The PSC2 has 2 UARTs (8250) as Mega Macro Function. PSC+80XH is used as the I/O address for this interface. Only TXD and DTR are outputted as UART signals from the PSC2.

UART3: PSC2+(800-807H)

UART4: PSC2+(808-80FH)

(9) Analog Touch Panel Interface

The PSC2 has a UART (8250) as Mega Macro Function. PSC+81XH is used as the I/O address for this interface. TXD, RXD, DTR, and CTS are inputted and outputted as UART signals from the PSC2.

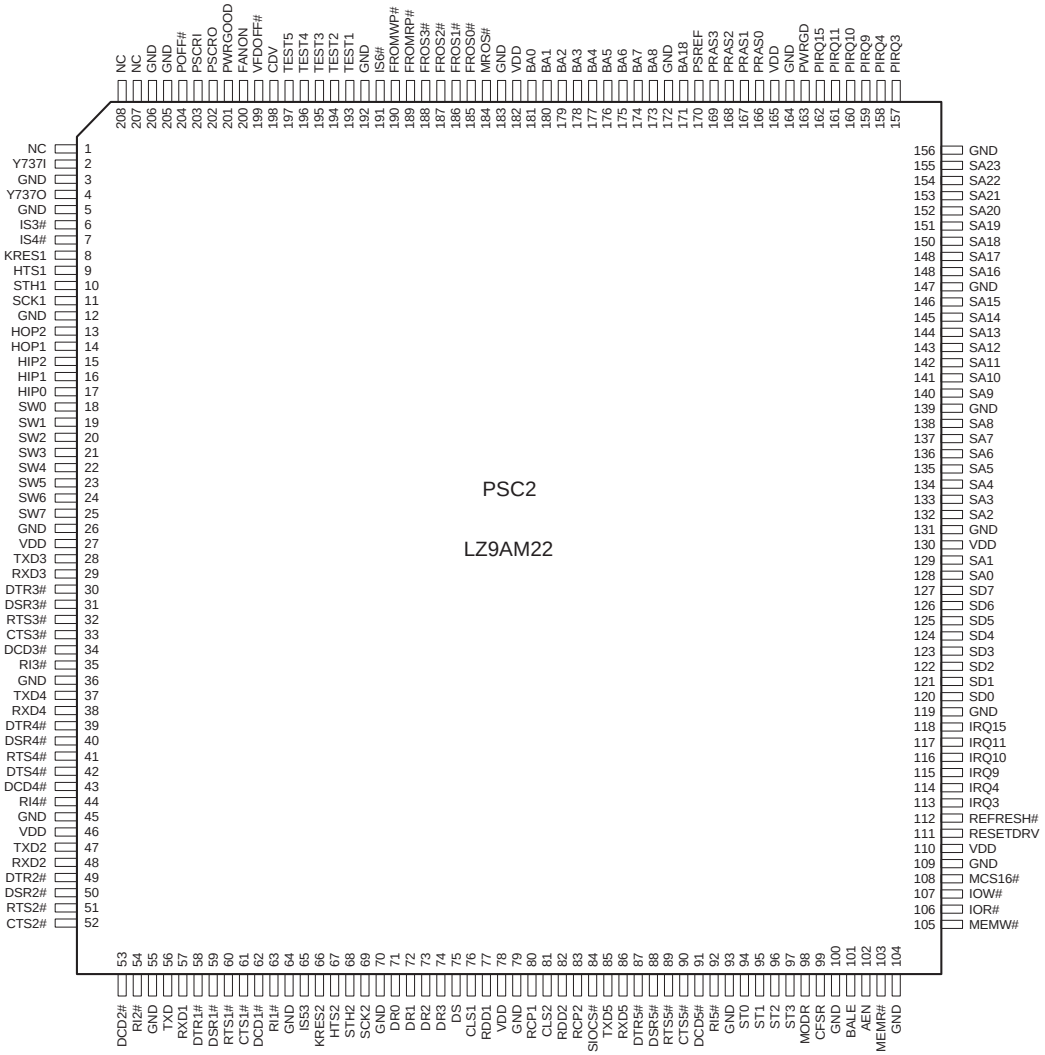
UART5: PSC2+(810-817H)

(10) General Purpose I/O Port

A 6-bit I/O port used for general purposes is configured in the PSC.

(11) Mode Key Control and Clerk Key Control (NotUsed)

17-4. PIN ASSIGNMENT



17-5. PIN DESCRIPTION

Pin No.	I/O	Signal name	Function
1		NC	
2	I	Y737I	SERAMIC RESONATOR CLOCK INPUT
3		GND	
4	O	Y737O	SERAMIC RESONATOR CLOCK OUTPUT
5		GND	
6	I	IS3#	STD CKDC INTERRUPT REQUEST (KIRQ1#)
7	I	IS4#	STD CKDC SHIFT ENABLE (SHEN1#)
8	O	KRES1	STD CKDC RESET
9	O	HTS1	STD CKDC HOST TO SUB
10	I	STH1	STD CKDC SUB TO HOST
11	O	SCK1	STD CKDC CLOCK
12		GND	
13	O	HOP2	GENERAL-PURPOSE OUTPUT PORT 2
14	O	HOP1	GENERAL-PURPOSE OUTPUT PORT 1
15	I	HIP2	GENERAL-PURPOSE INPUT PORT 2
16	I	HIP1	GENERAL-PURPOSE INPUT PORT 1
17	I	HIP0	GENERAL-PURPOSE INPUT PORT 0
18	I	SW0	DIP SWITCH 0
19	I	SW1	DIP SWITCH 1
20	I	SW2	DIP SWITCH 2
21	I	SW3	DIP SWITCH 3
22	I	SW4	DIP SWITCH 4
23	I	SW5	DIP SWITCH 5
24	I	SW6	DIP SWITCH 6
25	I	SW7	DIP SWITCH 7
26		GND	
27		VDD	
28	O	TXD3	RS-232 FRONT VFD TXD
29	I	RXD3	RS-232 FRONT VFD RXD
30	O	DTR3#	RS-232 FRONT VFD DTR
31	I	DSR3#	RS-232 FRONT VFD DSR
32	O	RTS3#	RS-232 FRONT VFD RTS
33	I	CTS3#	RS-232 FRONT VFD CTS
34	I	DCD3#	RS-232 FRONT VFD DCD
35	I	RI3#	RS-232 FRONT VFD RI
36		GND	
37	I	TXD4	RS-232 CUSTOMER VFD TXD
38	I	RXD4	RS-232 CUSTOMER VFD RXD
39	O	DTR4#	RS-232 CUSTOMER VFD DTR
40	I	DSR4#	RS-232 CUSTOMER VFD DSR
41	O	RTS4#	RS-232 CUSTOMER VFD RTS
42	I	CTS4#	RS-232 CUSTOMER VFD CTS
43	I	DCD4#	RS-232 CUSTOMER VFD DCD
44	I	RI4#	RS-232 CUSTOMER VFD RI
45		GND	
46		VDD	
47	O	TXD2	RS-232 COM4/6 TXD
48	I	RXD2	RS-232 COM4/6 RXD
49	O	DTR2#	RS-232 COM4/6 DTR
50	I	DSR2#	RS-232 COM4/6 DSR
51	O	RTS2#	RS-232 COM4/6 RTS
52	I	CTS2#	RS-232 COM4/6 CTS
53	I	DCD2#	RS-232 COM4/6 DCD
54	I	RI2#	RS-232 COM4/6 RI
55		GND	
56	O	TXD1	RS-232 COM3/5 TXD
57	I	RXD1	RS-232 COM3/5 RXD
58	O	DTR1#	RS-232 COM3/5 DTR
59	I	DSR1#	RS-232 COM3/5 DSR
60	O	RTS1#	RS-232 COM3/5 RTS
61	I	CTS1#	RS-232 COM3/5 CTS
62	I	DCD1#	RS-232 COM3/5 DCD
63	I	RI1#	RS-232 COM3/5 RI
64		GND	
65	I	S5#	OPT CKDC SHIFT ENABLE (SHEN2#)
66	O	KRES2	OPT CKDC RESET
67	O	HTS2	OPT CKDC HOST TO SUB
68	I	STH2	OPT CKDC SUB TO HOST
69	O	SCK2	OPT CKDC CLOCK
70		GND	
71	O	DR0	DRAWER DRIVE 0
72	O	DR1	DRAWER DRIVE 1
73	O	DR2	DRAWER DRIVE 2
74	O	DR3	DRAWER DRIVE 3
75	I	DS	DRAWER OPEN SENSOR
76	I	CLS1	MCR CARD LOADING SIGNAL 1
77	I	RDD1	MCR READ DATA 1
78		VDD	
79		GND	
80	I	RCP1	MCR READ CLOCK PULS 1
81	I	CLS2	MCR CARD LOADING SIGNAL 2
82	I	RDD2	MCR READ DATA 2
83	I	RCP2	MCR READ CLOCK PULS 2
84	O	SIOCS#	SUPER I/O A15-A11 DECODE
85	O	TXD5	RS-232 TUCH PANEL TXD
86	I	RXD5	RS-232 TUCH PANEL RXD
87	O	DTR5#	RS-232 TUCH PANEL DTR
88	I	DSR5#	RS-232 TUCH PANEL DSR
89	O	RTS5#	RS-232 TUCH PANEL RTS
90	I	CTS5#	RS-232 TUCH PANEL CTS
91	I	DCD5#	RS-232 TUCH PANEL DCD
92	I	RI5#	RS-232 TUCH PANEL RI
93		GND	
94	O	ST0	MODE KEY/CLERK KEY STROBE 0
95	O	ST1	MODE KEY/CLERK KEY STROBE 1
96	O	ST2	MODE KEY/CLERK KEY STROBE 2
97	O	ST3	MODE KEY/CLERK KEY STROBE 3
98	I	MODR	MODE KEY RETURN
99	I	CFSR	CLERK KEY RETURN
100		GND	
101	I	BALE	ISA BUS ADDRESS LATCH ENABLE from CPU
102	I	AEN	ISA ADDRESS ENABLE from CPU
103	I	MEMR#	ISA MEMORY READ COMMAND from CPU

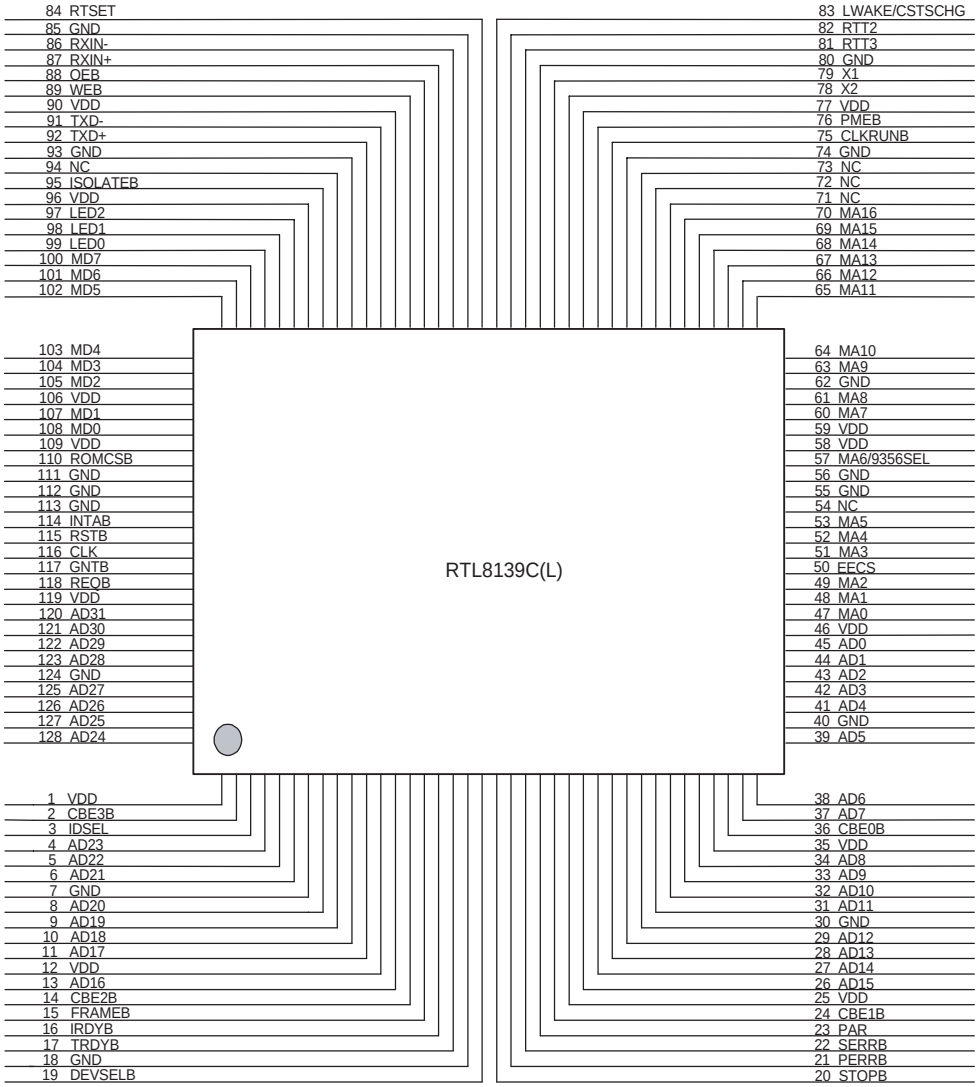
Pin No.	I/O	Signal name	Function
104		GND	
105	I	MEMW#	ISA MEMORY WRITE COMMAND from CPU
106	I	IOR#	ISA I/O READ COMMAND from CPU
107	I	IOW#	ISA I/O WRITE COMMAND from CPU
108	O	MCS16#	MEMORY CHIP SELECT 16 to CPU
109		GND	
110		VDD	
111	I	RESETDRV	ISA SYSTEM RESET from CPU
112	I	REFRESH#	ISA D-RAM REFRESH from CPU
113	I	IRQ3	ISA INTERRUPT REQUEST 3 from ISA
114	I	IRQ4	ISA INTERRUPT REQUEST 4 from ISA
115	I	IRQ9	ISA INTERRUPT REQUEST 9 from ISA
116	I	IRQ10	ISA INTERRUPT REQUEST 10 from ISA
117	I	IRQ11	ISA INTERRUPT REQUEST 11 from ISA
118	I	IRQ15	ISA INTERRUPT REQUEST 15 from ISA
119		GND	
120	I/O	SD0	ISA BUS D0
121	I/O	SD1	ISA BUS D1
122	I/O	SD2	ISA BUS D2
123	I/O	SD3	ISA BUS D3
124	I/O	SD4	ISA BUS D4
125	I/O	SD5	ISA BUS D5
126	I/O	SD6	ISA BUS D6
127	I/O	SD7	ISA BUS D7
128	I	SA0	ISA BUS SA0
129	I	SA1	ISA BUS SA1
130		VDD	
131		GND	
132	I	SA2	ISA BUS SA2
133	I	SA3	ISA BUS SA3
134	I	SA4	ISA BUS SA4
135	I	SA5	ISA BUS SA5
136	I	SA6	ISA BUS SA6
137	I	SA7	ISA BUS SA7
138	I	SA8	ISA BUS SA8
139		GND	
140	I	SA9	ISA BUS SA9
141	I	SA10	ISA BUS SA10
142	I	SA11	ISA BUS SA11
143	I	SA12	ISA BUS SA12
144	I	SA13	ISA BUS SA13
145	I	SA14	ISA BUS SA14
146	I	SA15	ISA BUS SA15
147		GND	
148	I	SA16	ISA BUS SA16
149	I	SA17	ISA BUS SA17
150	I	SA18	ISA BUS SA18
151	I	SA19	ISA BUS SA19
152	I	SA20	ISA BUS SA20
153	I	SA21	ISA BUS SA21
154	I	SA22	ISA BUS SA22
155	I	SA23	ISA BUS SA23

Pin No.	I/O	Signal name	Function
156		GND	
157	O	PIRQ3	INTERRUPT REQUEST 3 to CPU
158	O	PIRQ4	INTERRUPT REQUEST 4 to CPU
159	O	PIRQ9	INTERRUPT REQUEST 8 to CPU
160	O	PIRQ10	INTERRUPT REQUEST 10 to CPU
161	O	PIRQ11	INTERRUPT REQUEST 11 to CPU
162	O	PIRQ15	INTERRUPT REQUEST 15 to CPU
163	O	PWRGD	
164		GND	
165		VDD	
166	O	PRAS0	STD PS RAM WORD CHIP SELECT 0
167	O	PRAS1	OPT PS-RAM WORD CHIP SELECT 1
168	O	PRAS2	OPT PS RAM WORD CHIP SELECT 2
169	O	PRAS3	OPT PS RAM WORD CHIP SELECT 3
170	O	PSREF	PS RAM READ/REFRESH
171	O	BA18	BIOS ROM BASE ADDRESS 18
172		GND	
173	O	BA8	BANK ADDRESS 8
174	O	BA7	BANK ADDRESS 7
175	O	BA6	BANK ADDRESS 6
176	O	BA5	BANK ADDRESS 5
177	O	BA4	BANK ADDRESS 4
178	O	BA3	BANK ADDRESS 3
179	O	BA2	BANK ADDRESS 2
180	O	BA1	BANK ADDRESS 1
181	O	BA0	BANK ADDRESS 0
182		VDD	
183		GND	
184	O	MROS#	MASK ROM CHIP SELECT
185	O	FROS0#	STD FLASH ROM CHIP SELECT
186	O	FROS1#	OPT FLASH ROM 1 CHIP SELECT
187	O	FROS2#	OPT FLASH ROM 2 CHIP SELECT
188	O	FROS3#	OPT FLASH ROM 3 CHIP SELECT
189	O	FROMRP#	FLASH ROM RESET/POWER DOWN
190	O	FROMWP#	FLASH ROM WRITE PROTECT
191	I	IS6#	FLASH ROM READY/BUSY- (FROMBY#)
192		GND	
193	I	TEST1	TEST PIN 1
194	I	TEST2	TEST PIN 2
195	I	TEST3	TEST PIN 3
196	I	TEST4	TEST PIN 4
197	I	TEST5	TEST PIN 5
198	I	CDV	TEST PIN CDV (1:NORMAL 0:TEST)
199	O	VFDOFF#	VFD OFF
200	O	FANON	FAN ON/STANDBY INDICATOR ON-
201	I	PWRGOOD	5V POWER GOOD
202	O	PSCRO	TEST RESET OUT
203	I	PSCRI	TEST RESET IN
204	I	POFF#	ACL INPUT from PS UNIT
205		GND	
206		GND	
207		NC	
208		NC	

18. LAN CONTROLLER

RealTak's RTL8139C is used.

18-1. PIN ASSIGNMENTS



18-2. PIN DISCRIPTION

1) POWER MANAGEMENT/ISOLATION INTERFACE

Symbol	Type	Pin No	Description
PMEB (PME#)	O/D	76	Power Management Event: Open drain, active low. Used by the RTL8139C(L) to request a change in its current power management state and/or to indicate that a power management event has occurred.
ISOLATEB (ISOLATE#)	I	95	Isolate pin: Active low. Used to isolate RTL8139C(L) from the PCI bus. The RTL8139C(L) does not drive its PCI outputs (excluding PME#) and does not sample its PCI input (including RST# and PCICLK) as long as Isolate pin is asserted.
LWAKE/ CSTSCHG	O	83	LAN WAKE-UP signal (When CardB_En=0, bit2 Config3): This signal is used to inform mother-board to execute wake-up process. The motherboard must support Wake-On-LAN (WOL). There are 4 choices of output, including active high, active low, positive pulse, and negative pulse, that may be asserted from the LWAKE pin. Please refer to LWACT bit in CONFIG1 register and LWPTN bit in CONFIG4 register for the setting of this output signal. The default output is an active high signal. Once there is a PME event having come in, the LWAKE and PMEB assert at the same time when the LWPME (bit4, CONFIG4) is set to 0. If the LWPME is set to 1, the LWAKE asserts only when the PMEB asserts and the ISOLATEB is low. CSTSCHG signal (When CardB_En=1, bit2 Config3): This signal is used in CardBus application only and is used to inform motherboard to execute wake-up process whenever there is PME event occurs. This is always an active high signal, the setting of LWACT (bit 4, Config1), LWPTN (bit2, Config4), and LWPME (bit4, Config4) means nothing in this case. This pin is a 3.3V signaling output pin.

2) PCI INTERFACE

Symbol	Type	Pin No	Description
AD31-0	T/S	120-123, 125-128, 4-6, 8-11, 13, 26-29, 31-34, 37-39, 41-45	PCI address and data multiplexed pins.
C/BE3-0	T/S	2, 14, 24, 36	PCI bus command and byte enables multiplexed pins.
CLK	I	116	Clock provides timing for all transactions on PCI and is input to PCI device.
CLKRUNB	I/O	75	Clock Run: This signal is used by RTL8139C(L) to request starting (or speeding up) the clock, CLK. CLKRUNB also indicates the clock status. For RTL8139C(L), CLKRUNB is an open drain output and also an input. The RTL8139C(L) requests the central resource to start, speed up, or maintain the interface clock by the assertion of CLKRUNB. For the host system, it is an S/T/S signal. The host system (central resource) is responsible for maintaining CLKRUNB asserted, and for driving it high to the negated (deasserted) state.
DEVSELB	S/T/S	19	Device Select: The RTL8139C(L) asserts this signal low when it recognizes its target address after FRAMEB is asserted. As a bus master, the RTL8139C(L) samples this signal to insure that a PCI target recognizes the destination address for the data transfer.
FRAMEB	S/T/S	15	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAMEB is asserted to indicate a bus transaction is beginning. While FRAMEB is asserted, data transfers continue. When FRAMEB is deasserted, the transaction is in the final data phase.
GNTB	I	117	Grant: This signal is asserted low to indicate to the RTL8139C(L) that the central arbiter has granted the ownership of the bus to the RTL8139C(L).
REQB	T/S	118	Request: The RTL8139C(L) will assert this signal low to request the ownership of the bus to the central arbiter.
IDSEL	I	3	Initialization Device Select is used as a chip-select during configuration read and write transactions.
INTAB	O/D	114	INTAB is used to request an interrupt.
IRDYB	S/T/S	16	Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction.
TRDYB	S/T/S	17	Target Ready indicates the target agent's ability to complete the current phase of the transaction.
PAR	T/S	23	Parity is even parity across AD31-0 and C/BE3-0.
PERRB	S/T/S	21	Parity Error: When the RTL8139C(L) is the bus master and a parity error is detected, the RTL8139C(L) asserts both SERR bit in ISR and Configuration Space command bit 8 (SERRB enable). Next, it completes the current data burst transaction, then stops operation and resets itself. After the host clears the system error, the RTL8139C(L) continues its operation. When the RTL8139C(L) is the bus target and a parity error is detected, the RTL8139C(L) asserts this PERRB pin.
SERRB	O/D	22	System Error: If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, RTL8139C(L) asserts both SERRB pin and bit 14 of Status register in Configuration Space.
STOPB	S/T/S	20	Stop: Indicates the current target is requesting the master to stop the current transaction.
RSTB	I	115	Reset: When RSTB is asserted low, the RTL8139C(L) performs internal system hardware reset. RSTB must be held for a minimum of 120 ns periods.

3) FLASH/EEPROM INTERFACE

Symbol	Type	Pin No	Description
MA16-3	O	70-63, 61, 60, 57, 53-51	Boot PROM address bus: These pins are used to access up to 128k-byte flash memory or EPROM.
MA8	I/O	61	Output pin as part of Boot PROM(or Flash) address bus after PCI reset. Input pin as Aux. Power detect pin to detect if Aux. Power exists or not, when initial power-on or PCI reset is asserted. Besides connecting this pin to Boot PROM, it should be pulled high to the Aux. Power via a resistor to detect Aux. power. If this pin is not pulled high to Aux. Power, the RTL8139C(L) assumes there is no Aux. power exists. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to aux. power via a resistor.
MA6/9356SEL	I/O	57	When this pin is pulled high with a 10K [resistor, the 93C56 EEPROM is used to store the resource data and CIS for the RTL8139C(L). The RTL8139C(L) latches the status of this pin at power-up to determine what EEPROM(93C46 or 93C56) is used, afterwards, this pin is used as MA6.
MA2/EESK	O	49	The MA2-0 pins are switched to EESK, EEDI, EEDO in 93C46 (93C56) programming or auto-load mode.
MA1/EEDI	O	48	
MA0/EEDO	O, I	47	
EECS	O	50	93C46 (93C56) chip select

Symbol	Type	Pin No	Description
MD0-7	I/O	108, 107, 105-100	Boot PROM data bus
ROMCSB	O	110	ROM Chip Select: This is the chip select signal of the Boot PROM.
OEB	O	88	Output Enable: This enables the output buffer of the Boot PROM or Flash memory during a read operation.
WEB	O	89	Write Enable: This signal strobes data into the Flash memory during a write cycle.

4) POWER PINS

Symbol	Type	Pin No	Description
VDD	P	1, 12, 25, 35, 46, 58, 59, 77, 90, 96, 106, 109, 119	+3.3V
GND	P	7, 18, 30, 40, 55, 56, 62, 74, 80, 85, 93, 111, 112, 113, 124	Ground

5) LED INTERFACE

Symbol	Type	Pin No	Description
LED0, 1, 2	O	99, 98, 97	LED pins LEDS1-0 / 00 / 01 / 10 / 11 LED0 / TX/RX / TX/RX / TX / TX LED1 / LINK100 / LINK10/100 / LINK10/100 / LINK100 LED2 / LINK10 / FULL / RX / LINK10 During power down mode, the LED's are OFF.

6) ATTACHMENT UNIT INTERFACE

Symbol	Type	Pin No	Description
TXD+ TXD-	O O	92 91	100/10BASE-T transmit (Tx) data.
RXIN+ RXIN-	I I	87 86	100/10BASE-T receive (Rx) data.
X1	I	79	25 MHz crystal/OSC. input.
X2	O	78	Crystal feedback output. This output is used in crystal connection only. It must be left open when X1 is driven with an external 25 MHz oscillator.

7) TEST AND THE OTHER PINS

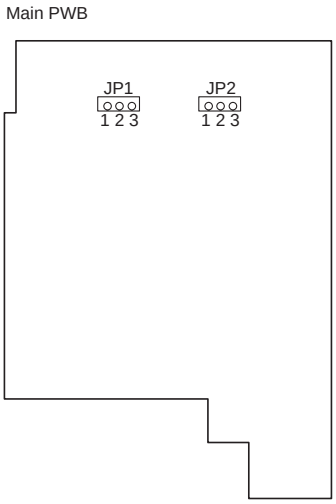
Symbol	Type	Pin No	Description
RTT2-3	TEST	81, 82	Chip test pins.
RTSET	I/O	84	This pin must pull low by 1.8KW resistor.
NC	–	54, 71, 72, 73, 94	Reserved

19. SYSTEM SWITCH

19-1. JUMPER SWITCH

For Jumper Switch, switched signals are read by PSC2 in the hardware.

Giving a meaning to it is up to the software.



JP1

Function	OFF (value=1)	ON (value=0)
COM3 IRQ assign	COM3=IRQ11	COM3=IRQ4

JP2

Function	OFF (value=1)	ON (value=0)
CMOS Initialize	Not Initialize	Initialize

JP0 (Fixed)

Function	OFF (value=1)
Serial3 decode mode	COM3

19-2. SPECIAL SYSTEM REGISTER 0 : 07F0H

SSR0	7	6	5	4	3	2	1	0
Read	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
Write	D7	D6	D5	D4	D3	D2	D1	D0

Read

bit7: SW7=JP0 (G/A Serial3 decode mode)

bit6: SW6=JP1 (COM3 IRQ assign)

bit5: SW5=Not use (Floppy Disk Controller)

bit4: SW4=Not use (Drive A: Device)

bit3: SW3=Not use (Boot Drive)

bit2: SW2=Not use (Drive C:, D: & E: Setting)

bit1: SW1=Not use (Drive C:, D: & E: Setting)

bit0: SW0=JP2 (CMOS Initialize)

Since pins except for SW0 16.7 are pulled up, the level is "1" when they are read.

Write

bit7-0: MD7-0=53h PSC2 Relocatable internal I/O access and SSR0 (07F0h) Read and SSR1 (07F1h) Read/Write allow

MD7-0><53h PSC2 Relocatable internal I/O access and SSR0 (07F0h) Read and SSR1 (07F1h) Read/Write inhibit (Default)

20. SYSTEM MEMORY

Two 168pin DIMM Sockets are provided.

20-1. STANDARD MEMORY

16777216 word×64bit SDRAM Registered DIMM (Installed)

Single 3.3V(±0.3V) Power Supply
Access time: PC100 or Higher
Refresh: 4096 cycles/64ms(15.625us)

Serial Presence Detect with EEPROM (SPD) support

Error Check & Collect memory (ECC) support

20-2. OPTIONAL MEMORY

16777216 word×64bit SDRAM Registered DIMM (Max)

Single 3.3V(±0.3V) Power Supply
Access time: PC100 or Higher
Refresh: 4096 cycles/64ms(15.625us)

Serial Presence Detect with EEPROM (SPD) support

Error Check & Collect memory (ECC) support

21. BIOS ROM

Atmel's Flash memory (AT49F040) is used.

5224,288 words x 8bit

22. ANALOG TOUCH PANEL

22-1. OUTLINES

Controlled by Fujitsu control IC (N010-0559-V021). Commands are given through the Serial Interface from the CPU.

Light Load Input Type

Communication Mode:	Full Duplex Communication Mode, Serial Interface
Transmission Speed:	9600bps
Data Transmission System:	Asymmetrical Advance Synchronization
Signal Level:	TTL Level
Data Format:	Binary
Bit Format:	Start bit (1) + Data bit (8) + Stop bit (1), non-parity
Interface Signal:	RXD/TXD
Sampling Speed:	100pps max.

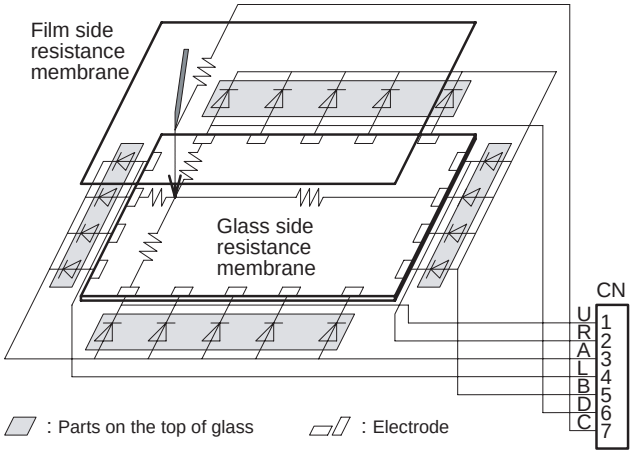
22-2. TOUCH PANEL CONTROL

UART5 included in PSC2 as Mega Macro Function is used. The I/O address for this interface is PSC2 + (810h-817h) = 990h-997h.

Command (CPU->Controller)

Command	Function	Code	Ope-code	Response		
				End Code	Coordinate Code	Notification Data
RESET	Controller initialization	80h	0	○	×	×
COLD-RST	Coordinate initialization	81h	0	○	×	×
STOP	Coordinate data send inhibit	82h	0	○	×	×
START	Coordinate data send resume	83h	0	○	×	×
CAL-IN	Correction start	84h	9	○	×	×
CAL-OUT	Correction complete	85h	4	○	×	×
CAL-SET	Previous data are set to Correction point.	86h	0	○	×	×
CANSEL	Correction interrupt	87h	0	○	×	×
REPORT	Controller state inquiry	88h	0	○	×	○
DIAG	Self diag execution	89h	1	○	×	×
SET-TIME	Timer setup after Pen Up	8Ah	1	○	×	×
SET-RATE	Sampling interval setup	8Bh	1	○	×	×
WRITE	Write to E2PROM	8Ch	3	○	×	×
READ	Read from E2PROM	8Dh	1	○	×	○
—	Reserve	8Eh	|	—	—	—
—	Reserve	8Fh	|	—	—	—
CALTRN	Transmits the correction coefficient to CPU.	E0h	1	○	×	×
CALRCV	Transmits the correction coefficient to this controller.	E1h	170	○	×	○
DUMY	Dummy Data for Sleep Cancel	FFh	0	—	—	—
— Pen Down —		—	—	×	○	×

22-3. TOUCH PANEL



Pin#	Signal	Memo
1	U	A/D Converter(Y-axis start point electrode voltage monitor)
2	R	A/D Converter (X-axis start point electrode voltage monitor)
3	A	Y-axis detection power
4	L	A/D Converter (X-axis end point electrode voltage monitor)
5	B	X-axis detection power
6	D	A/D Converter (Y-axis end point electrode voltage monitor)
7	C	A/D Converter (Touch coordinate detection)

23. SHUTDOWN CONTROL

The power switch of the UP-5900 is used to switch between terminal ON state and stand-by state.

When starting the terminal, the power switch should be set to ON. When the power switch is set to the stand-by mode, the power unit is automatically terminated. By holding HOP1 pin of PSC by the software (PHOLD =1), the power unit does not stop, but keeps ON until the software cancels holding.

If shutdown control cannot be made by the above software, turn ON the shutdown switch on the side to forcibly cancel the stand-by mode. When, however, the power switch is ON, though the shutdown switch is turned ON, the power unit will ignore it and will not stop.

Sense Register of power ON/OFF control and power switch state

General-use I/O Port (PSC+408h)=588h

HIOP	b7	b6	b5	b4	b3	b2	b1	b0
Read	0	BLON	PHOLD	SLEEP	0	0	PHSNS	MLOCK
Write	0	BLON	PHOLD	SLEEP	0	0	0	0

bit7 : not use

bit6 : LCD Back Light ON signal

BLON=0 : LCD Back Light is turned off.

BLON=1 : LCD Back Light is turned on.

bit5 : AC power Hold signal

PHOLD="0" When Power Switch is at OFF position, the power is shut down.

PHOLD="1" Though Power Switch is at OFF position, the power is kept on.

PHOLD, Default is "0." To inhibit manual power OFF operation of Power Switch after POWER ON, set to "1."

When it is set to "0," the power can be turned off by manual operation of Power Switch.

bit7 : not use

This bit is designed for prevention of power OFF by manual operation of Power Switch, and it has no effect on power interruption by power service interruption.

bit4 : SLEEP=0 Operation Mode Rotates the power fan, and connects the LCD power.

SLEEP=1 Sleep Mode Stops the power fan, and shuts down the LCD power.

In the UP-5000 series, SLEEP=0 should be always kept.

bit3-2 : not use

bit1 : Power Switch state Sense Register

PHSNS="0" Power Switch OFF

PHSNS="1" Power Switch ON

bit0 : not use (CPU cooler Motor LOCK sense)

(MLOCK=0 Motor rotating)

(MLOCK=1 Motor stationary)

24. VACUUM FLUORESCENT DISPLAY (VFD)

24-1. UP-P20DP/UP-I20DP

(1) Outlines

Display content: 5 × 7dots (20 Digits × 2 Lines) + Period + Comma + ▽

UART4 in PSC2 is used as Serial6.

(RS-232C Level I/F, Serial, 8bit, non-parity, 1stop-bit, 9600bps, RXD/DSR/DTR)

Automatic blinking of ▽ mark when supplying the power.

(2) VFD Control

UART4 built in PSC2 as Mega Macro Function is used. The I/O address fir this interface is PSC2 + (808h-80Fh) = 908h-90Fh.

(3) Command (CPU → Controller)

Command	Function	Code	
HT	Shift display position to right	09h	
BS	Shift display position to left	08h	
US LF	Shift display position up	1Fh 0Ah	
LF	Shift display position down	0Ah	
US CR	Shift display position to the end of the same line	1Fh 0Dh	
CR	Shift display position to left edge of the same line	0Dh	
HOM	Shift display position to home position	0Bh	
US B	Shift display position to bottom position	1Fh 42h	
US $ n m	Shift display position to any desired position	1Fh 24h	n m
CLR	Display clear	0Ch	
CAN	Display line clear	18h	
US X n	Bright ness adjustment of luminescent display tube	1Fh 58h	n
US E n	Display blink	1Fh 45h	n
ESC @	Display initialization	1Bh 40h	
ESC t n	Selection of text code table	1Bh 74h	n
ESC R n	Selection of international text	1Bh 52h	n
US r n	Select/cancel of highlighted text	1Fh 72h	n
US MD1	Over-write Mode select	1Fh 01h	
US MD2	Vertical Scroll Mode select	1Fh 02h	

Command	Function	Code	
US MD3	Horizontal Scroll Mode select	1Fh 03h	
ESC & s n m [a [p] sua] (m-n+1)	Download text definition	1Bh 26h	s n m [a [p] sua] (m-n+1)
ESC ? n	Download text delete	1Bh 3Fh	n
ESC % n	Download text set select/cancel	1Bh 25h	n
ESC W n m x1 y1 x2 y2	Window range select/cancel	1Bh 57h	n m x1 y1 x2 y2
US :	Macro content definition start and end	1Fh 3Ah	
US ^ n m	Macro process execution	1Fh 5Eh	n m
US @	Self Test execution	1Fh 40h	
US v n	Status check by DTR signal	1Fh 76h	n
US T n h m	Counter (Time) setup and display	1Fh 54h	n h m
US U	Counter (Time) display	1Fh 55h	
US # n m	Annunciater display select	1Fh 23h	n m
SLP	Sleep Mode execution	06h	n
DC	Select position display blinking	17h	n m s
US . n	Period display select	1Fh 2Eh	n
US , n	Comma display select	1Fh 2Ch	n
US ; n	(Period+Comma) display select	1Fh 3Bh	n

For details of control codes, refer to “UP-P20DP Command Specifications.”

(4) Connector specifications

RJ45 (for UP-P20DP)

Pin No.	Signal	Function	I/O
1	+5V	+5V	—
2	ER	SLP control(Data terminal Ready)	O
3	SD	Send Data	O
4	SG	Signal Ground	—
5	SG	Signal Ground	—
6	(NC)	(Not Connected)	
7	DR	Data set Ready	I
8	+5V	+5V	—

Connector (for UP-I20DP)

Pin No.	Signal	Function	I/O
1	SG	Signal Ground	—
2	SG	Signal Ground	—
3	SD	Send Data	O
4	ER	SLP control(Data terminal Ready)	O
5	DR	Data set Ready	I
6	+5V	+5V	—
7	+5V	+5V	—

Note: The UP-P20DP and the UP-I20DP cannot be used at the same time because of limited power capacity.

25. DRAWER

25-1. OUTLINES

Operations of 2ch are allowed for the ER-03DW and the ER-04DW. However, simultaneous drive is not allowed.
Drawer drive time by PSC2 = 45ms
Time from PSC2 drive to sense becoming effective: Sense effective time = 200ms
When two drawers are opened continuously, the output interval of drawer open commands is 50ms or more.
The number of times of drawer open is limited to max. 15 times/min due to the power specification.

Drive shutdown function by PSC2 service interruption detection.

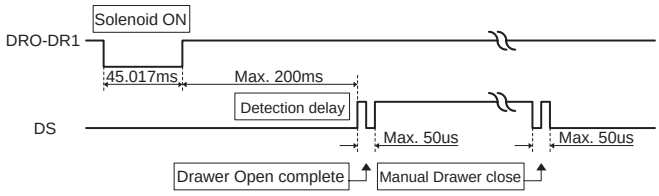
25-2. DRAWER CONTROL

Drawer Control Register (PSC+0Ah)=18Ah

DCR	b7	b6	b5	b4	b3	b2	b1	b0
Read	DS	0	0	0	1	1	DR1	DR0
Write	×	×	×	×	1	1	DR1	DR0

bit7 : Drawer open Sensor input port (Read Only)
DS=0 : All of drawers are closed.
DS=1 : One of drawers is opened.
bit6-4 : not use
bit3 : Drawer solenoid drive port 3 (not use)
bit2 : Drawer solenoid drive port 2 (not use)
bit1 : Drawer solenoid drive port 1
DR1=0 : Solenoid ON
DR1=1 : Solenoid OFF
bit0 : Drawer solenoid drive port 0
DR0=0: Solenoid ON
DR0=1: Solenoid OFF

25-3. TIMING CHART



26. MAGNETIC CARD READER (MCR)

26-1. OUTLINES

Targets are the UP-E12MR and the UP-E12MR2.

2ch MCR interface allows simultaneous read.

Each channel includes 96Byte FIFO.

26-2. CARD READ OPERATION

The MCR interface enters the stand-by state for card read when the following setup is made by the main CPU.
Mode set: Set to the mode corresponding to the card standard (JBA/ABA/IATA) to be handled.
Start mark set: Set to the start mark corresponding to each card standard.
Interruption reset: Since the card cannot be read under the active state of interruption, interruption is reset.

When the card is scanned, the MCR I/F converts serial data input from MCR into parallel data. The converted data are written into the FIFO buffer character by character in the sequence of Start Mark to LRC. The FIFO buffer has the capacity of 96Byte. The number of characters of the card corresponding to each standard is as shown below:

JBA (JIS2 type) : FMax. 72 Character(8bit/Character)

ABA (JIS2 Type No. 2 Track) : FMax. 40 Character(5bit/Character)

IATA (JIS1 Type No. 1 Track) : FMax. 79 Character(7bit/Character)

One FIFO is provided for each of two channel interfaces, and simultaneous read is allowed in the MCR connection corresponding to JBA/ABA or IATA/ABA.

When card scan is completed, the MCR interface interruption is made active.
The main CPU reads the card data taken in interruption process from the FIFO buffer. Read from the main CPU is allowed by IN command of No Wait.
Even after reading the last character LCR, the FIFO buffer has 10 - 20 characters of “0”. Therefore, when the last data LCR is read, the FIFO should be reset before making the next card Read Enable.

In the MCR interface, the next cars is not read until the interruption is reset from the main CPU.

27. SERIAL PORT

27-1. OUTLINES

D-SUB 9pin Connector COM1 and COM2 are standard provisions.

In addition, 1 channel of RJ-45 8pin Connector COM port is provided.

To supply +5V power, CI signal of COM1/COM2 and +5V power can be switched.

27-2. CONNECTOR SPECIFICATIONS

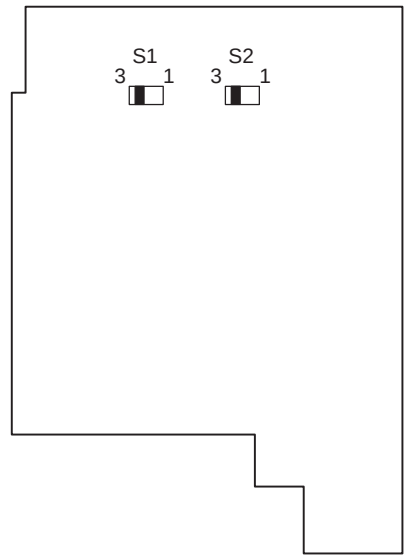
(1) COM1 & COM2

D-SUB9

Pin No.	Signal	Function	I/O
1	CD	Data Carrier Detect	I
2	RD	Receive Data	I
3	SD	Send Data	O
4	ER	Data Terminal Ready	O
5	SG	Signal Ground	—
6	DR	Data set Ready	I
7	RS	Request to Send	O
8	CS	Clear to Send	I
9	CI/+5V	Ring Indicate / +5V	I/–

CI and +5V are switched by the Switch.

Main PWB



S2=COM1 : 1=+5V
3=CI
S1=COM2 : 1=+5V
3=CI

(2) COM3/5

RJ45

Pin No.	Signal	Function	I/O
1	RS	Request to Send	O
2	ER	Data terminal Ready	O
3	SD	Send Data	O
4	SG/(+5V)	Signal Ground / (+5V)	—
5	SG	Signal Ground	—
6	RD	Receive Data	I
7	DR	Data set Ready	I
8	CS	Clear to Ssend	I

+5V can be supplied to 4pin by switch of Pattern Cut & Jumper connection. (Default = SG)

CHAPTER 6. BIOS SETUP UTILITY

1. OUTLINE

In UP-5900, there is a utility that rewrites minimum required setup information at the system boot up that resides in ROM-BIOS.

Setup data is undefined at the first system startup, so setup must be done. Basically, just doing initial setting in setup can do system operation.

Also, BIOS in UP-5900 will automatically detects memory size / HDD, which makes no need for running setup again after changing hardware (expanding memory, changing HDD, etc).

However, adding / removing second HDD will require running menu format setup.

2. STARTING PROCEDURE

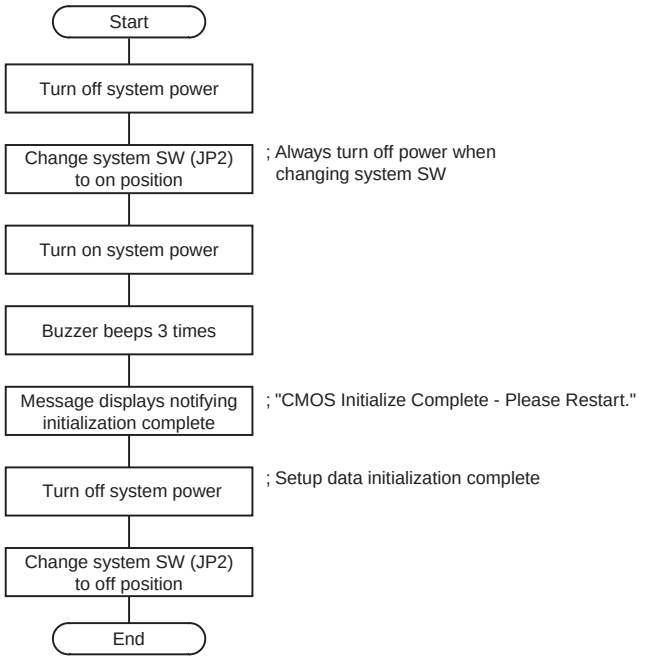
There are 2 ways of starting setup, changing system SW and connecting PS/2 type full keyboard. Setup started by each procedure will be as follows.

Procedure for running setup	Setup contents
Start with system SW	• Setup data initialization.
Start with full keyboard	• Setup data initialization. • Running setup in menu format.

2-1. STARTING SETUP BY CHANGING SYSTEM SW

Setup data initialization will be processed when system is started with system SW (JP2) turned on.

Following shows the flow of this procedure.



2-2. STARTING SETUP WITH FULL KEYBOARD

Starting and operating setup with full keyboard will require UP-C30PK, PS/2 type full keyboard.

In this setup will use only numpad.

Procedure for starting setup is as follows.

(1) Start the system.

(2) On numpad, press period key when as following message appears on screen.

"SETUP Available"

(3) If bios accepts above key, as following message appears on screen.

"Entering SETUP..."

(4) Press following keys according to setup wanted while "Waiting SETUP Entry Key ..." message appears on screen.

- Do setup initialization

  → On numpad, press 8 and period at continuously.

  Buzzer beeps 3 times and "CMOS Initialize Complete - Please Restart." message appears on screen. After this message, turn off system power

- Starting setup in menu format

  → On numpad, press 7 and period at continuously.

  After 1 beep, menu will be displayed.

3. SETUP OUTLINE IN MENU FORMAT

Setup in menu format is not required during normal operation. Use only in case such as checking contents of setup during maintenance, or modifying setup contents required due to system operation.

3-1. KEY ASSIGNMENTS

Following num keys are used during operation of setup in menu format.

Key used	Functions
5	Display help
3 (Pg Dn)	Change setting (reverse)
9 (Pg Up)	Change setting (forward)
7 (Home)	Initialize all category displayed
1 (End)	Return to previous value
8 (↑)	Change category (up)
2 (↓)	Change category (down)
4 (←)	Change menu (left)
6 (→)	Change menu (right)
. (Del)	Select submenu, confirm, execute
0 (Ins)	End, return from submenu

Setup in the menu format displays key assignment described in the lower 2 lines. There is a case where [Continue] and [OK] are displayed during help and in some settings. In this case, press arbitrary key to go to next step.

Press period when [Press Enter] is displayed.

4. SETUP MENU

Setup menu is as follows.

Main

Item	Initial Value	Description & Note
System Time	00:00:00	Set System Time for battery backup RTC. Setting format is (HH:MM:SS). If RTC data is undefined, clock is initialized to 00:00:00
System Date	01/01/2002	Set System Date. Set System Date for battery backup RTC. Setting format is (MM/DD/YYYY). If RTC data is undefined, clock is initialized to 2002-01-01.
Legacy Diskette A:	Enabled	Set enable/disable on internal FDD.
Primary Master	Auto	Set internal HDD type. By setting to Auto, default size of HDD is automatically detected at BIOS boot up.
Serial port A	Enabled	Set enable/disable on COM1.
Serial port B	Enabled	Set enable/disable on COM2.
Parallel port	Enabled	Set enable/disable on LPT1.
Mode	Bi-Directional	Set LPT1 Mode. Can configurable [Output only], [Bi-Directional],[EPP],[ECP]. Use [Bi-Directional] until announced by RETAILING SYSTEMS DEVELOPMENT DEPARTMENT.

Boot

Item	Initial Value	Description & Note
Boot Device Priority	FD/IDE Devices	Set boot device priority. Don't change this setting until announced by RETAILING SYSTEMS EVELOPMENT DEPARTMENT.

Exit

Item	Description
Exit Save Changes	System reset after save SETUP value to CMOS RAM.
Exit Discard Changes	Discard all changes and System reset.
Load SETUP Defaults	Load SETUP defaults to CMOS RAM.
Discard Changes	Discard all changes.
Save Changes	Save SETUP value to CMOS RAM.

CHAPTER 7. HDI RECOVERY PROCEDURES (For VK version)

1. GENERAL

This manual describes the procedures to recover the UP-5900 hard disk image (HDI) to factory setup state.

There are two ways to recover for the UP-5900.

① Recovery by CD boot with CD drive (SCSI-connection) which has bootable BIOS

② Recovery by FD boot with bootable FD, USB-CD or SCSI-connection CD

Refer to “3. Recovery procedures with SCSI card/USB-CD device” to select which way to recover.

Procedure ① is simple to perform, because only Recovery CD-ROM is used for recovering.

If CD booting is not available, use procedure ②, In this case, a boot FD must be prepared by referring to “5. Creating bootable FD for recovering HDI.”

2. REQUIRED ITEMS

- SCSI card + CD-ROM drive or USB-CD

  (The driver must support DOS and CD-ROM drive must be able to read CD-R format.
  For USB-CD, it is recommended to use one with an AC adapter.)
- UP-5900 Product Recovery CD-ROM
- Keyboard
- 1.44MB floppy disk (Not required for CD booting)

3. RECOVERY PROCEDURES WITH SCSI CARD / USB-CD DEVICE

Adaptec AHA-2940AU (*1)	CD boot recovery Refer to “6. Recovery procedures.”
Adaptec AHA-2910 series, etc. without boot BIOS	FD boot recovery (1) Refer to “5. Creating bootable FD for recovering HDI” to create a bootable FD for recovery. (2) Refer to “6. Recovery procedures” to perform recovery with the bootable FD.
USB-CD (*2)	
Adaptec AHA-2930U/ AHA-2930U2 (*1)	FD boot recovery (1) Refer to “5. Creating bootable FD for recovering HDI” to make a bootable FD for recovery. (2) Refer to “6. Recovery procedures” to perform recovery with the bootable FD. (Note: Be careful not to boot from CD.)
SCSI with boot BIOS, made by other than Adaptec	

*1: The boot area of “UP-5900 Product Recovery CD-ROM” includes following ASPI drivers which are included in Windows98.

ASPI8DOS.SYS (Ver.1.32S)
ASPI8U2.SYS (Ver.1.00S)

Above drivers can be used for PCI I/F SCSI card from Adaptec (AHA-2940AU and AHA-2910 series), but cannot be used for AHA-2930U/AHA-2930U2. To use AHA-2930U/AHA-2930U2, driver file ASPI8DOS.SYS (Ver.1.35 or later) /ASPI8U2.SYS (Ver.1.03 or later) is required. (According to Adaptec support information)

*2: Checked device: CD-210PU by TEAC

4. PRECAUTIONS

- Use of the UP-5900 Product Recovery CD-ROM is limited to the UP-5900. Never use it for other POS or PC.
- All files in the UP-5900 Product Recovery CD-ROM must be used only for recovering UP-5900 hard disk image. Modification of any file in the UP-5900 Product Recovery CD-ROM that is not described in this manual is forbidden.
- SCSI or USB-CD to be used must support DOS drivers.
- Before executing recovery, be sure to back up all necessary files to other media. When recovery is executed, all data in hard disk will be deleted.
- When a SCSI device with bootable BIOS is used, system will boot from SCSI device instead of UP-5900 FD/HDD due to boot device priority. To avoid this, boot from FD first, and then insert UP-5900 Product Recovery CD-ROM into SCSI CD drive.
- Be careful to avoid breaker OFF or power failure during the recovery procedure.
- When using USB-CD, it is recommended to use AC adapter for stable power supply. Depending on device, it may be possible that power supply from USB bus power (5V) is not enough to perform stable readouts, resulting an error.

5. CREATING BOOTABLE FD FOR RECOVERING HDI

(1) Create a Windows98 startup disk.

Open [Startup Disk] tab in [Add/Remove Programs] from the control panel, and click [Create Disk] button. Follow the instructions shown on the display.

(2) Delete the following files from “Windows98 startup disk” created in the previous step.

(Files to be deleted)

ASPI2DOS.SYS
ASPI4DOS.SYS
ASPICD.SYS
ASPI8DOS.SYS
ASPI8U2.SYS
BTCDROM.SYS
BTDOSM.SYS
OAKCDROM.SYS
EBD.SYS(Hidden)
AUTOEXEC.BAT
CONFIG.SYS
SETRAMD.BAT
README.TXT
FLASHPT.SYS
EXTRACT.EXE
DRVSPACE.BIN
EBD.CAB

(The following files must not be deleted.)

MSDOS.SYS (Hidden)

IO.SYS (Hidden)

COMMAND.COM

HIMEM.SYS

FINDRAMD.EXE

RAMDRIVE.SYS

FDISK.EXE

(3) Copy all files in [BOOT_FD] folder of the UP-5900 Product Recovery CD-ROM into root folder (A:\) of “Windows98 startup disk” prepared in the previous step.

[BOOT_FD] folder includes the following files:

CONFIG.SYS

AUTOEXEC.BAT

POSRCVR.BAT

SETRAMD_.BAT

POSCHK.EXE

MSCDEX.EXE

FORMAT.COM

ANSI.SYS

RAMDRV\HDDUMP.EXE

RAMDRV\MENU.TMU

RAMDRV\TMENU.COM

(4) Copy the driver for USB-CD or SCSI+CD into root folder of “Windows98 startup disk”.

(Example: When USB_CD”TEAC CD-210PU” is used:)

> COPY USB_CD.SYS A:\

(5) Use an editor to edit AUTOEXEC.BAT (2-4 lines) included in “Windows98 startup disk” and add your device driver for CD drive to be used. Set the CD logic drive name to “R:”

Autoexec.bat < Default >	
line2	rem Add your device driver for CD here.
line3	rem Set CD drive to R:drive.
line4	rem (Example) MSCDEX.EXE /D:MSCD001 /L:R

Autoexec.bat < When USB_CD”TEAC CD-210PU” is used >	
line2	rem Add your device driver for CD here.
line3	rem Set CD drive to R:drive.
line4	MSCDEX.EXE /D: USBCD001 /L:R

Note: All files included in CD-ROM have read-only attribute flag set. Clear the read-only attribute flag (which are copied from CD-ROM) to edit and save.

(6) Edit CONFIG.SYS (line 7-9) included in “Windows98 startup disk” to add your device driver for USB_CD or SCSI{CD drive to be used.

Config.sys < Default >		
line7	rem	Add your device driver for CD here.
line8	rem	(Exapmle) DEVICEHIGH=ASPI8DOS.SYS
line9	rem	DEVICEHIGH=ASPICD.SYS /D:MSCD001

Config.sys < When USB_CD”TEAC CD-210PU” is used >	
line7	rem Add your device driver for CD here.
line8	DEVICEHIGH=USB_CD.SYS /D:USBCD001
line9	

6. RECOVERY PROCEDURES

The procedures by FD boot and CD boot are described below. (The two procedures are same except for (1) and (5).)

∗When Product Recovery CD Utility is used, all data in the HDD will be deleted. Before executing recovery, be sure to save the necessary files to other media.

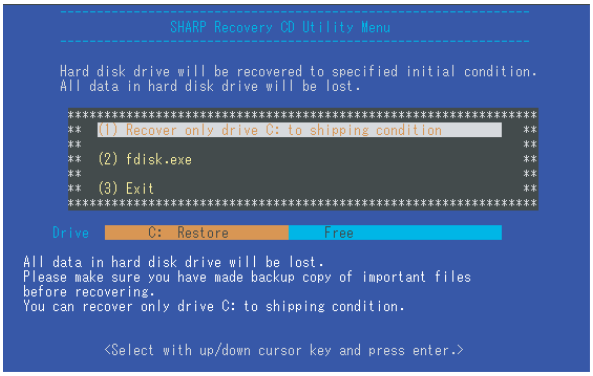
(1) [FD boot recovery]

Create a boot FD for recovery according to “5. Creating bootable FD for recoverying HDI.”

Connect the keyboard and USB-CD or SCSI+CD drive to UP-5900. Insert bootable FD for recovery into FD drive of UP-5900. Turn on the power of UP-5900. When menu as shown below is displayed, insert UP-5900 Product Recovery CD-ROM into CD drive.

[CD boot recovery]

Connect the keyboard, SCSI card and CD-ROM drive to UP-5900. Setup SCSI card and insert UP-5900 Product Recovery CD-ROM into CD drive, so that machine will be booted from the CD-ROM. The menu shown below is displayed.



(2) Confirm that “(1) Recover only drive C: to shipping condition” is selected and press Enter key.

The recovery CD utility menu shown below is displayed.



(3) When the Recovery CD Utility program is executed, all data in the hard disk will be deleted. Be sure to save the necessary files to other media before execution of recovery procedure. Press Enter key to start recovery procedure. Reconfirmation message shown below is displayed.

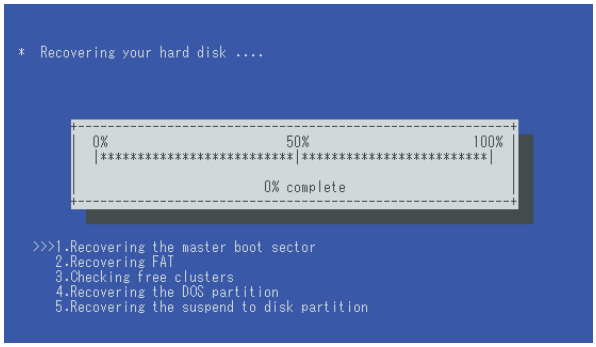


(4) Press [Y] key to start the recovery procedure.

When [Y] key is pressed, following messages are displayed and procedures are executed automatically in sequence.

1. Recovering the master boot sector
2. Recovering FAT
3. Checking free clusters
4. Recovering the DOS partition

There is no “suspend to disk partition” in UP-5900 HDI, so “5. Recovering the suspend to disk partition” will be skipped.



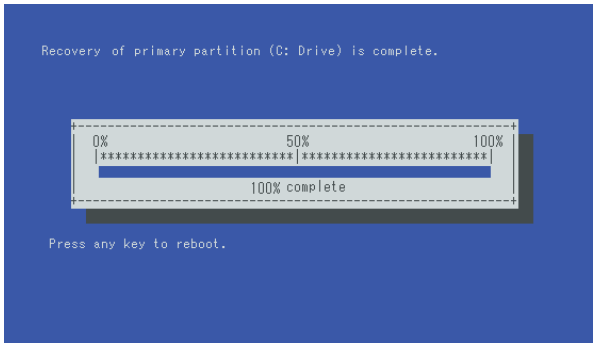
(5) When the Recovery CD Utility program is completed, following message as shown below is displayed.

[FD boot recovery]

Remove the UP-5900 Product Recovery CD-ROM from CD drive, and press Enter key to reboot from boot FD. (In the following steps, use only bootable FD and do not use UP-5900 Product Recovery CD-ROM.)

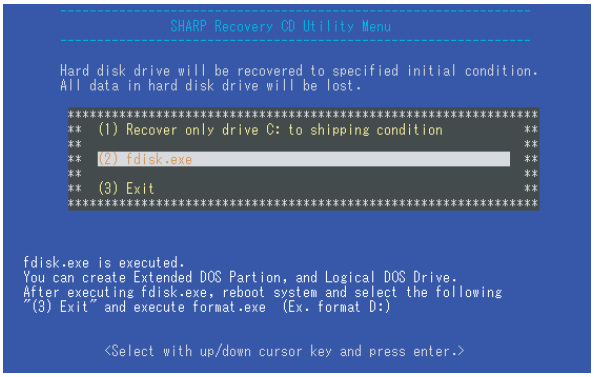
[CD boot recovery]

Press Enter key to reboot from CD.



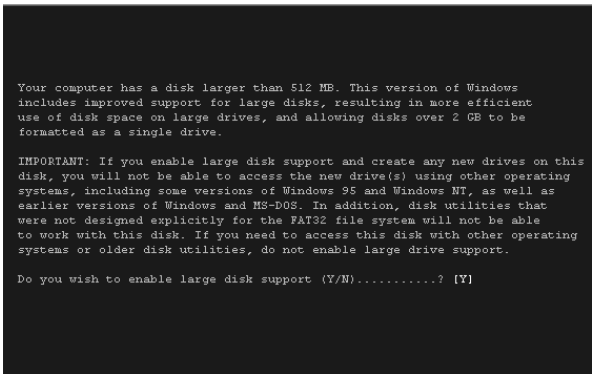
(6) The recovery menu is displayed.

Use [↑] [↓] keys to select “(2) fdisk.exe” and press Enter key.



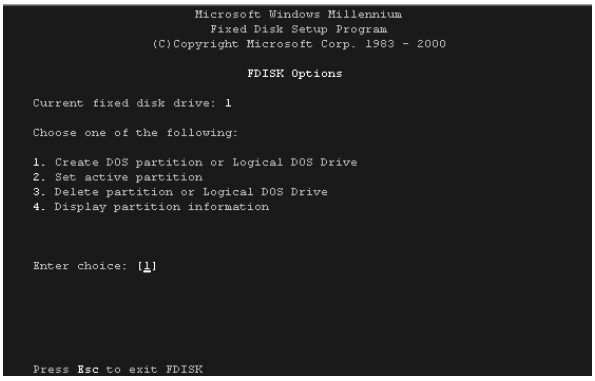
(7) “Fdisk.exe” is executed and menu shown below is displayed.

To enable large-capacity disk support, confirm that [Y] is selected and press Enter key.

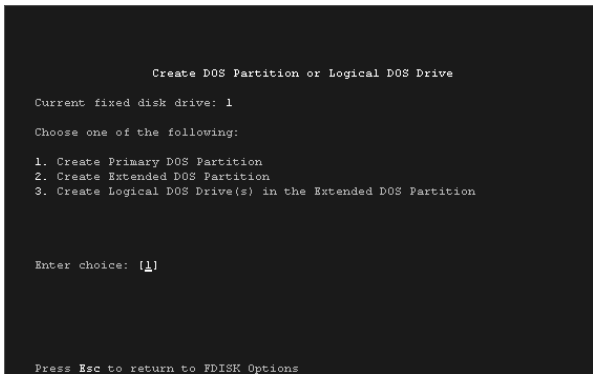


(8) “Fdisk Options” are displayed.

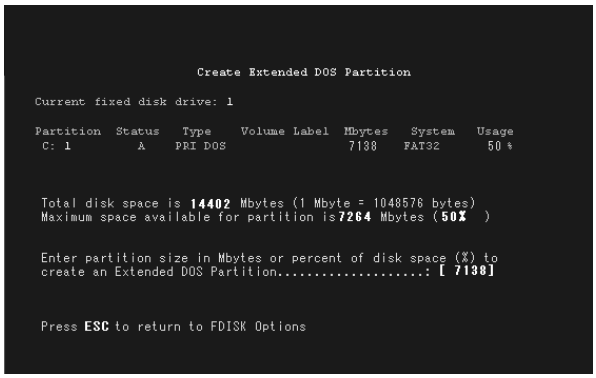
Select “1. Create DOS Partition or Logical DOS Drive” and press Enter key.



(9) Select “2.Create Extended DOS Partition” and press Enter key.

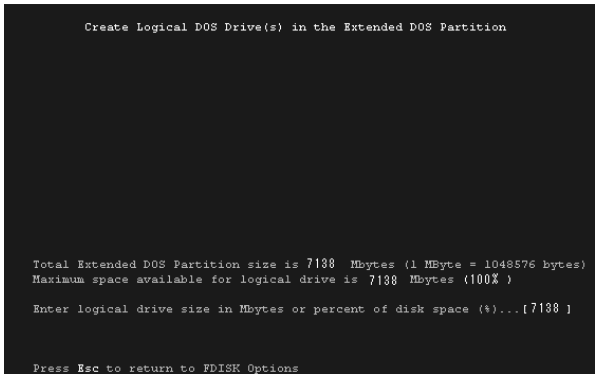


(10) Enter the extended DOS partition size. For 15GB HDD, enter “7138” and press Enter key to return to the factory default size.



(11) Press ESC key to proceed, and create the logical drive.

Enter the logical drive size and press Enter key. Logical drive will be created.

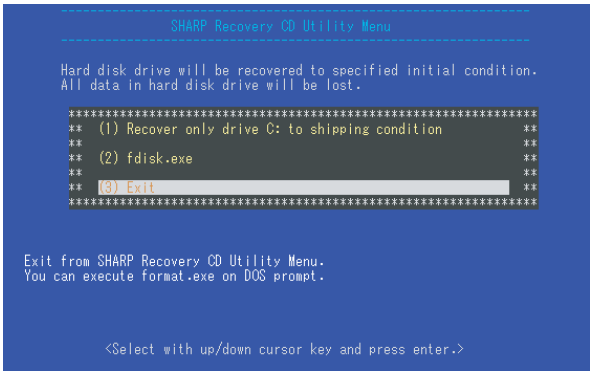


(12) After creating the logical drive (D:), press ESC key 3 times to exit from “fdisk.exe” command. After exiting from “fdisk.exe” command, press [Ctrl]{[Alt]{[Del] keys or turn UP-5900 power switch on/off to reboot.

(Since Fdisk.exe program from Windows98 is used, following message will be displayed, but please ignore the message.
Shut down Windows before restarting)

(13) When the machine is booted from boot FD or CD, the recovery menu is displayed. Use [↑] [↓] keys to select “(3) EXIT” and press Enter key to go back to DOS prompt. Format the logical drive (D:) created in the previous step.

Example: E\format D:



(14) After completion of formatting, turn off power for the UP-5900 and connected devices, and remove USB-CD or SCSI card/CD-ROM drive.

The hard disk recovery is now completed.

CHAPTER 8. ABOUT UTILITY SOFTWARE

The UP-5900's utility softwere are provided by SHARP.

1. TOUCH PANEL CALIBRATION UTILITY PROGRAM

[File name] : CALWINR. EXE

[Out line] : This utility is for aligning press position and display position.
This utility should be used to calibrate when following case is occurred.
When touch panel driver was set up.
When touch panel device was exchanged in case like service.
Calibration data are written in "EEPROM".
This utility is composed from the following screens.
The calibration screen which does calibration operation.
The drawing test screen which confirms a pressing position and displaying position in touch panel after calibration is finished.
CAUTION : A full keyboard is necessary to operate this utility.
Touch panel driver must be set up in order to run this utility.

[Function] : The position calibration for the touch panel.
To adjust it, use the touch pen of K-PAD (Keyboard enhanced Personal Digital Assistant).

PARTS CODE	PARTS NAME	MODEL
CPENP1004PCN5	Touch pen	K-PDA ZR-xxxx series

2. DOUBLE TAP SETUP UTILITY PROGRAM

[File name] : DBLTAP.EXE

[Out line] : Double tap setup utility DBLTAP.EXE (will call utility onward) is used to improve double tap control over touch panel.
This utility can visually customize double tap recognition speed and tolerance area.
Customized value will be saved independently to each user, and automatically reflected to touch panel operation.

[Function] : Configures tolerance distance for first tap and second tap upon double tap operation. (Area :Wide - Narrow)
Configures tolerance for time difference between first tap and second tap upon double tap operation. (Speed:Slow - Fast)

3. STAMP LOGO REGISTER UTILITY PROGRAM FOR POS PRINTER

[File name] : PRTUTIL.EXE

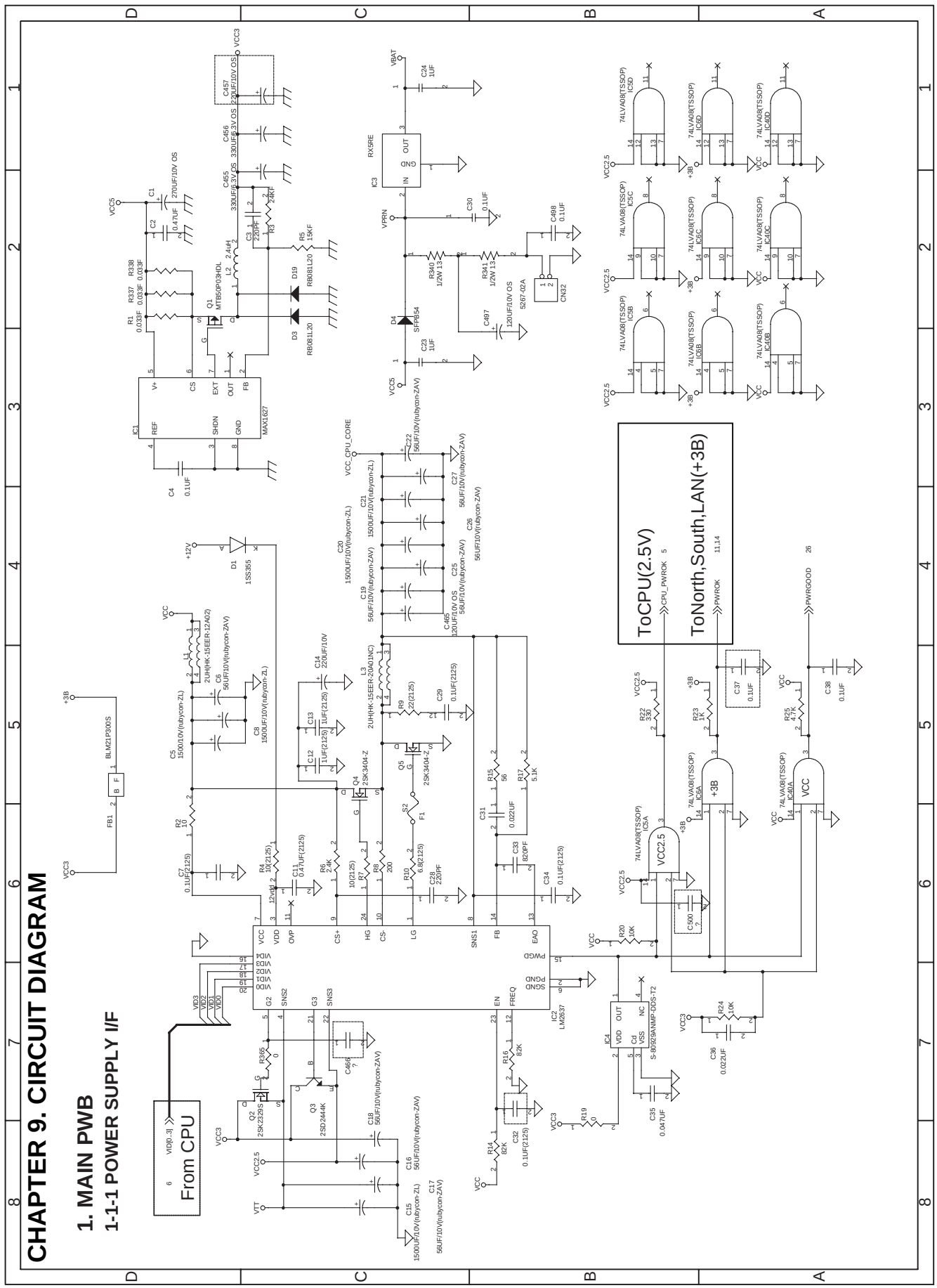
[Out line] : This utility registers stamp logo image to POS printer.
Supported printers are 2 types, UP-T80BP and ER-01PU.

[Function] : Registration of 2 types of logo image and test print for UP-T80BP.
Registration of 1 type of logo image and test print for ER-01PU.

CHAPTER 9. CIRCUIT DIAGRAM

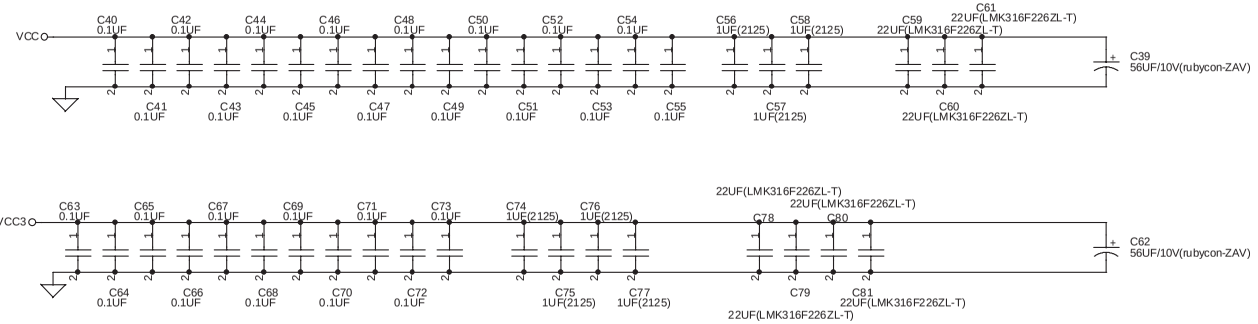
1. MAIN PWB

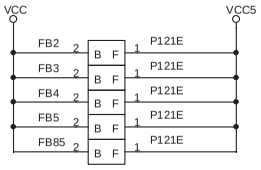
1-1-1 POWER SUPPLY I/F

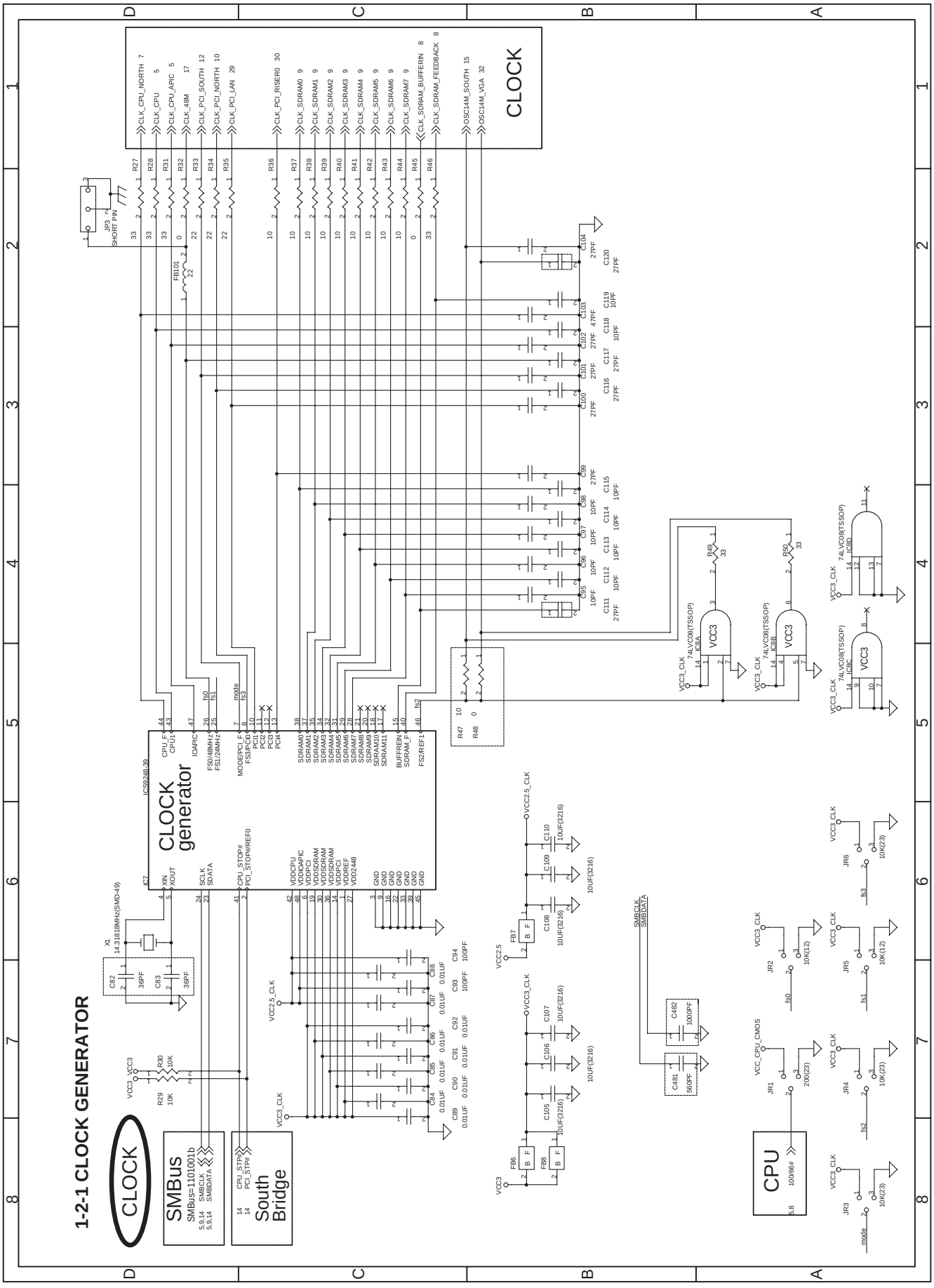


1-1-2 POWER SUPPLY I/F (CAP)

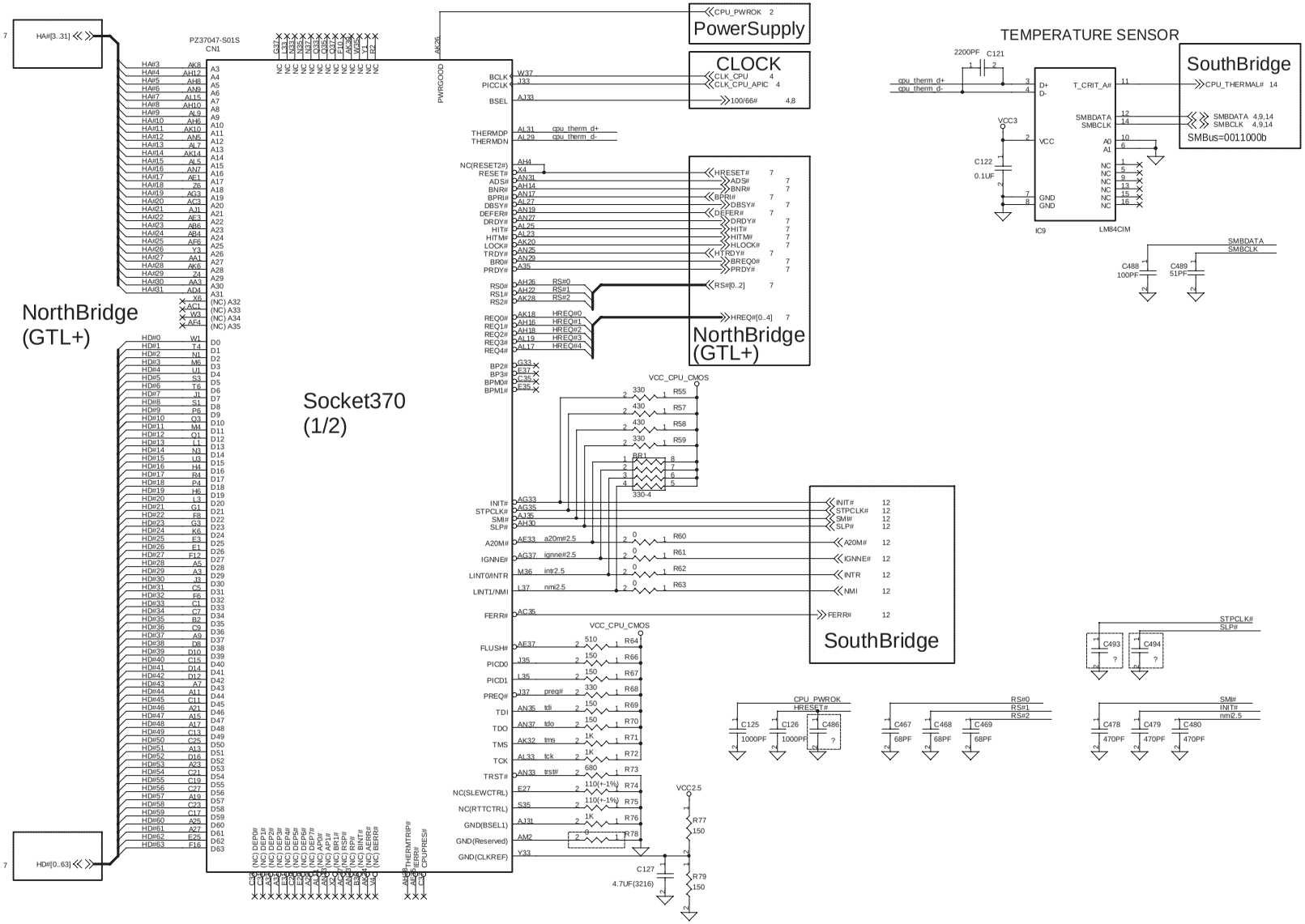
capacitor



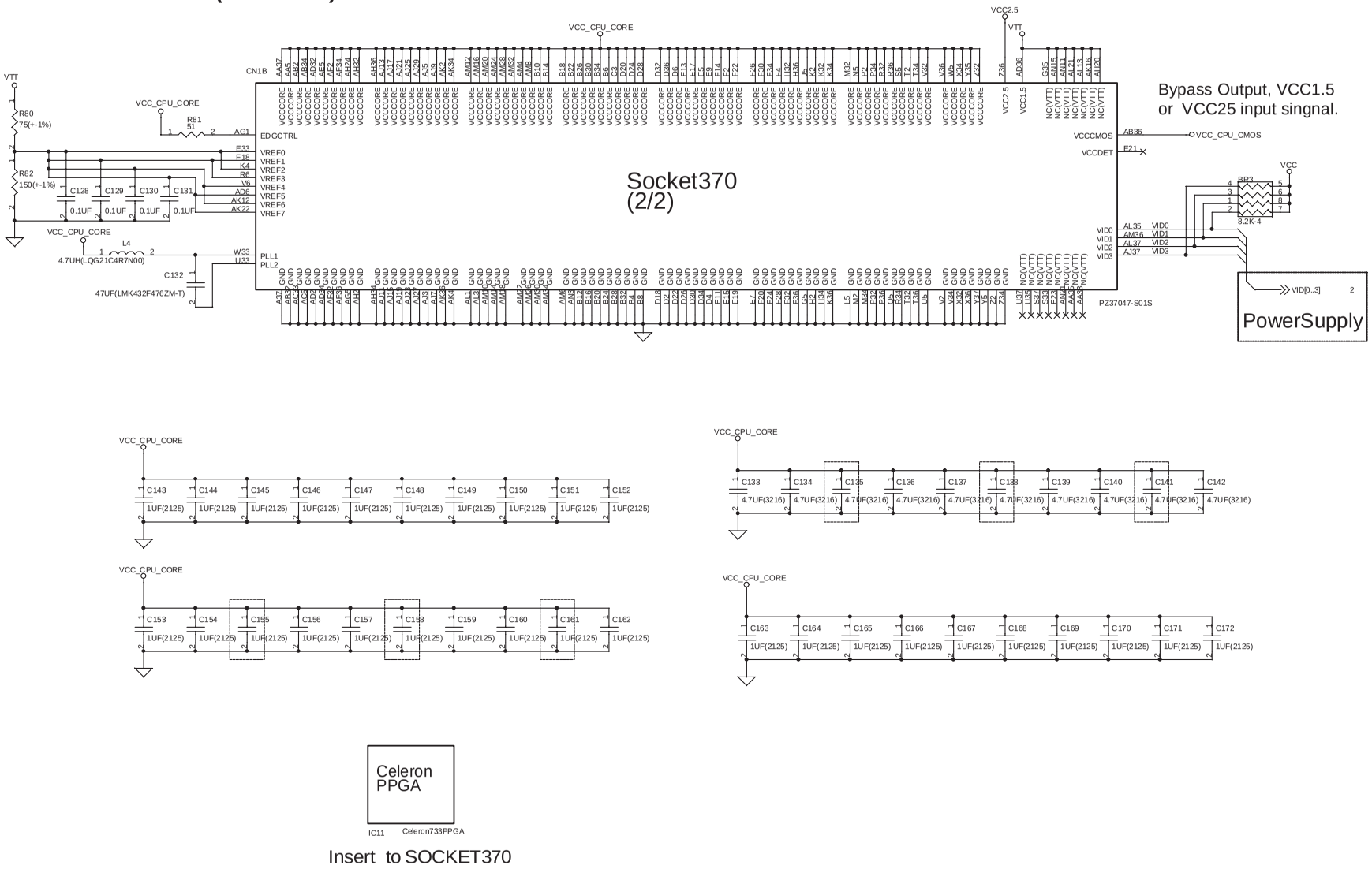


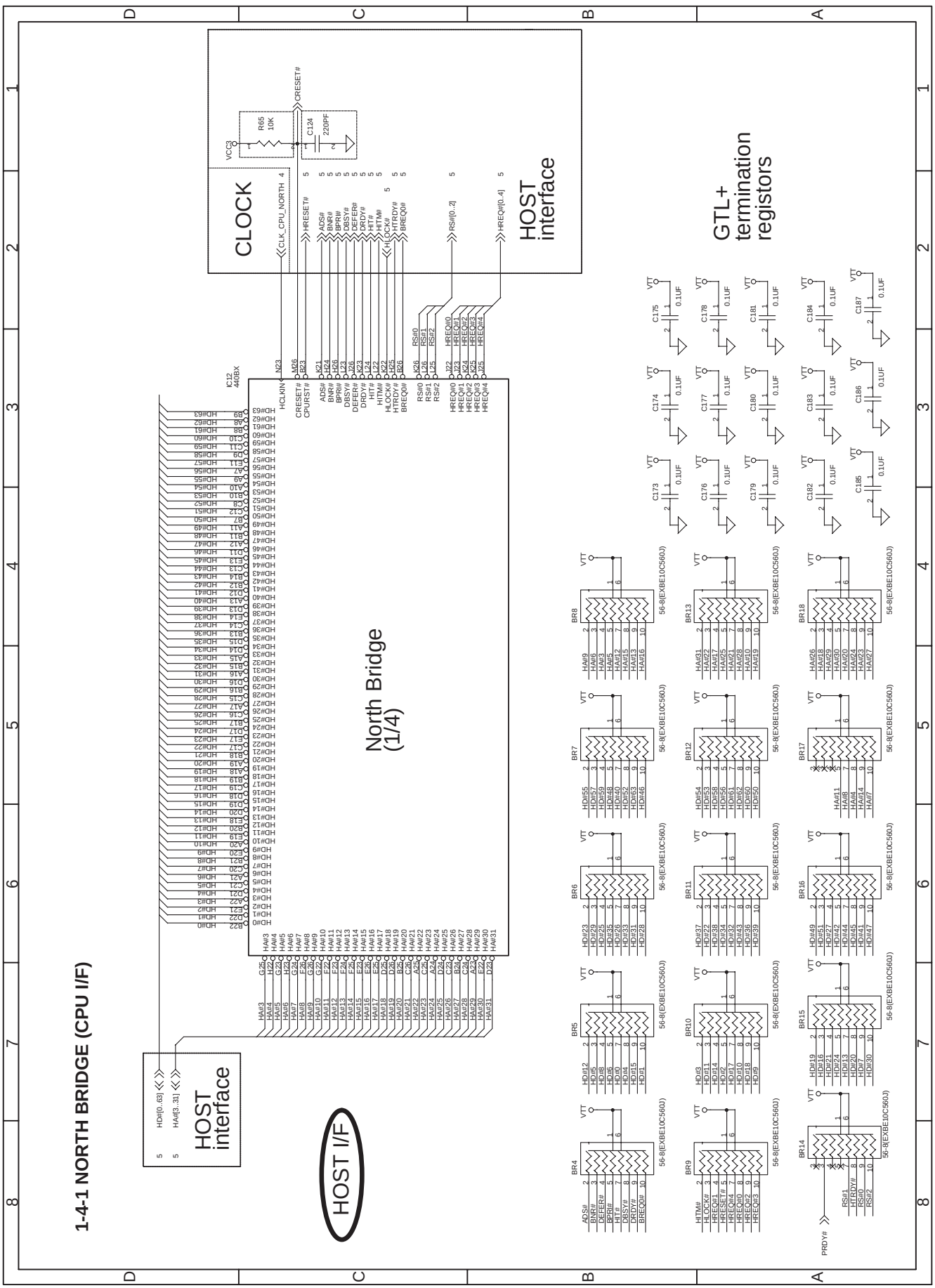

1-2-1 CLOCK GENERATOR
CLOCK
SMBus
SMBus=1101001b
South Bridge
CPU
CLOCK generator
ICS9248-39
CLOCK
CLK_CPU_NORTH
CLK_CPU
CLK_CPU_APIC
CLK_48M
CLK_PCI_SOUTH
CLK_PCI_NORTH
CLK_PCI_LAN
CLK_PCI_RISER0
CLK_SDRAM0
CLK_SDRAM1
CLK_SDRAM2
CLK_SDRAM3
CLK_SDRAM4
CLK_SDRAM5
CLK_SDRAM6
CLK_SDRAM7
CLK_SDRAM_BUFFERN
CLK_SDRAM_FEEDBACK
OSC14M_SOUTH
OSC14M_VGA
VCC3
VCC2.5
VCC3_CLK
VCC2.5_CLK
VCC_CPU_CMOS
SMBCLK
SMBDATA
74LVC08(TSSOP)
JP0
SHORT PIN
JR1
JR2
JR3
JR4
JR5
JR6
mode
fs0
fs1
fs2
fs3

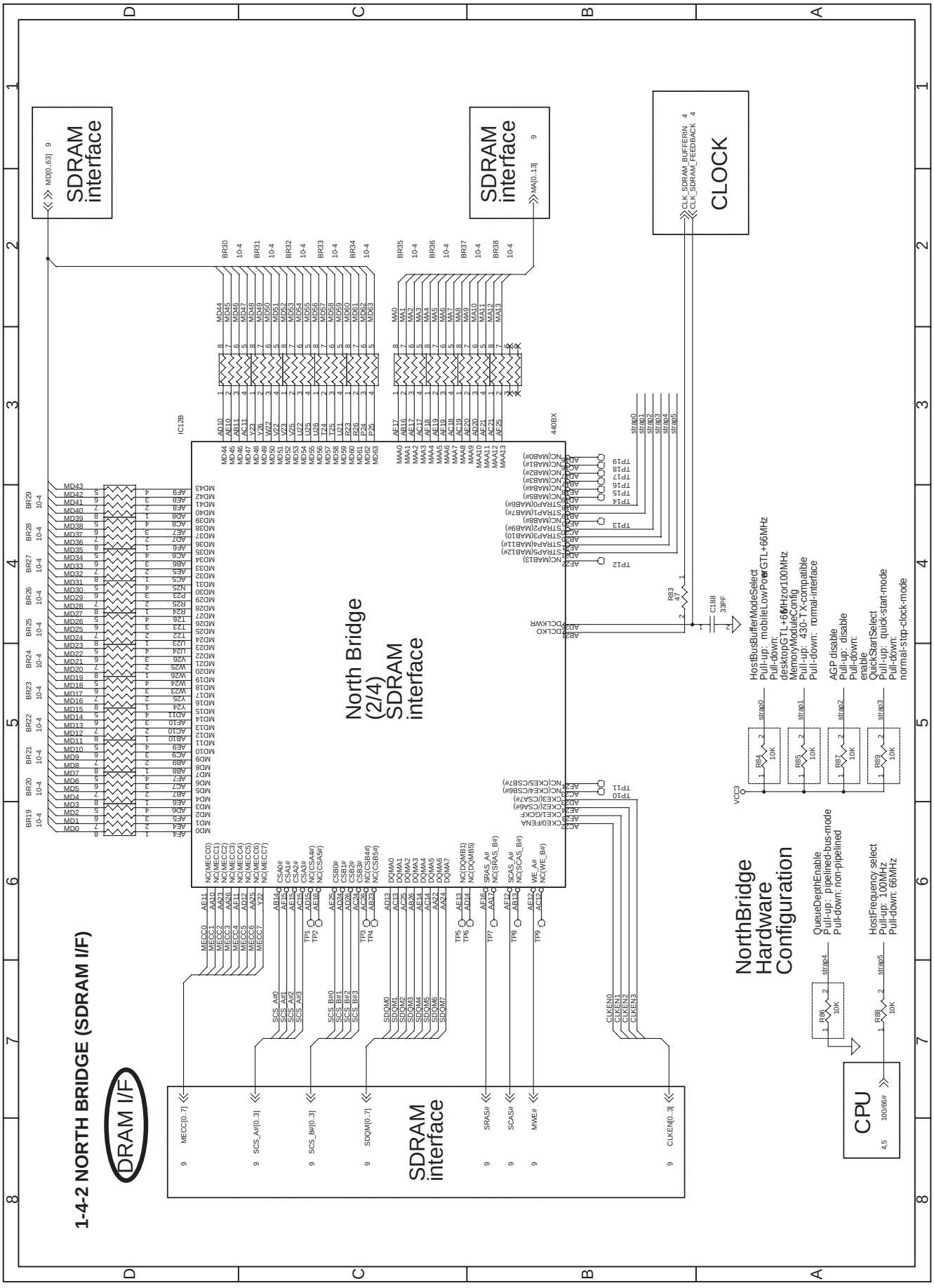
1-3-1 SOCKET 370 (CPU I/F)



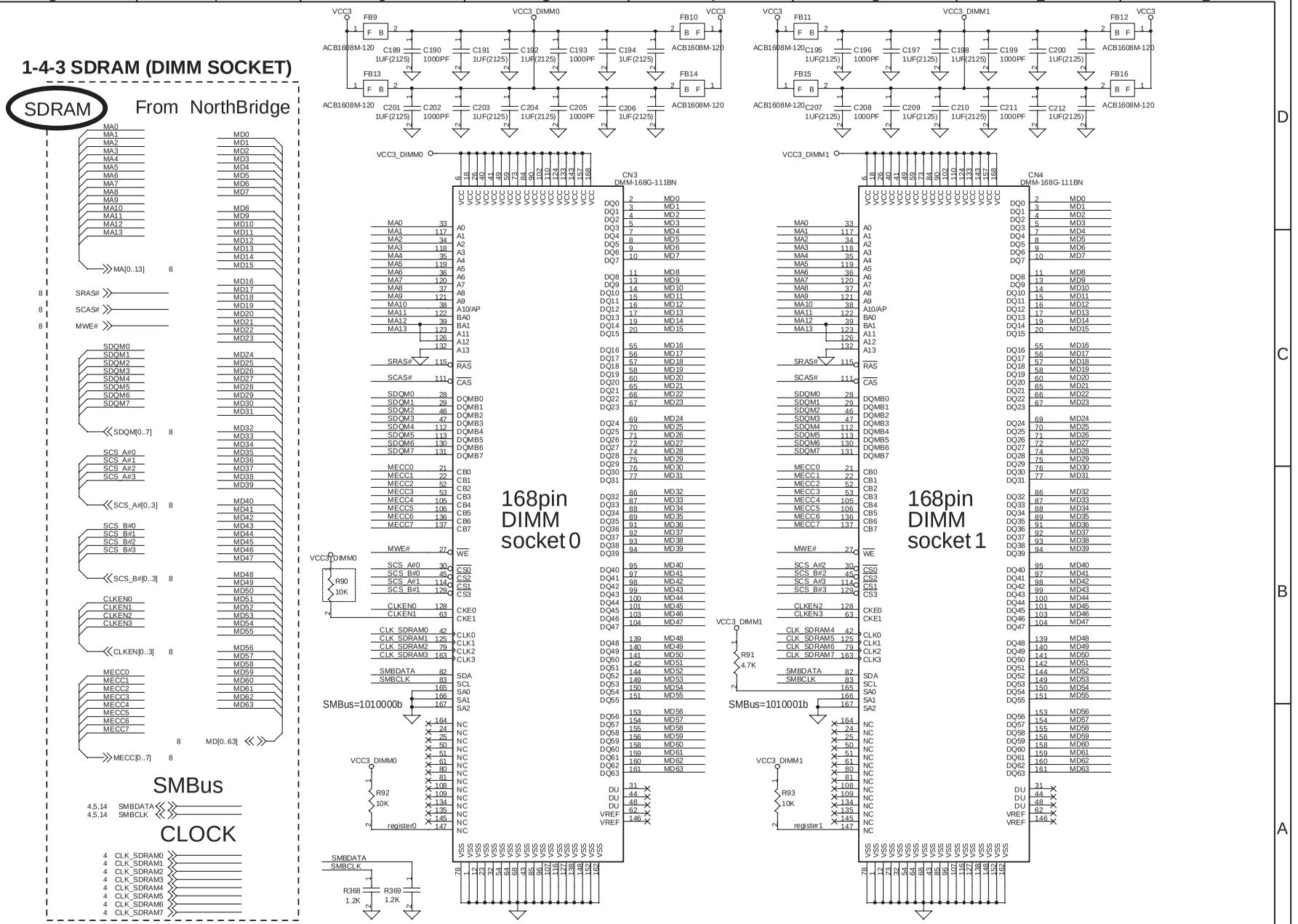
1-3-2 SOCKET 370 (POWER I/F)



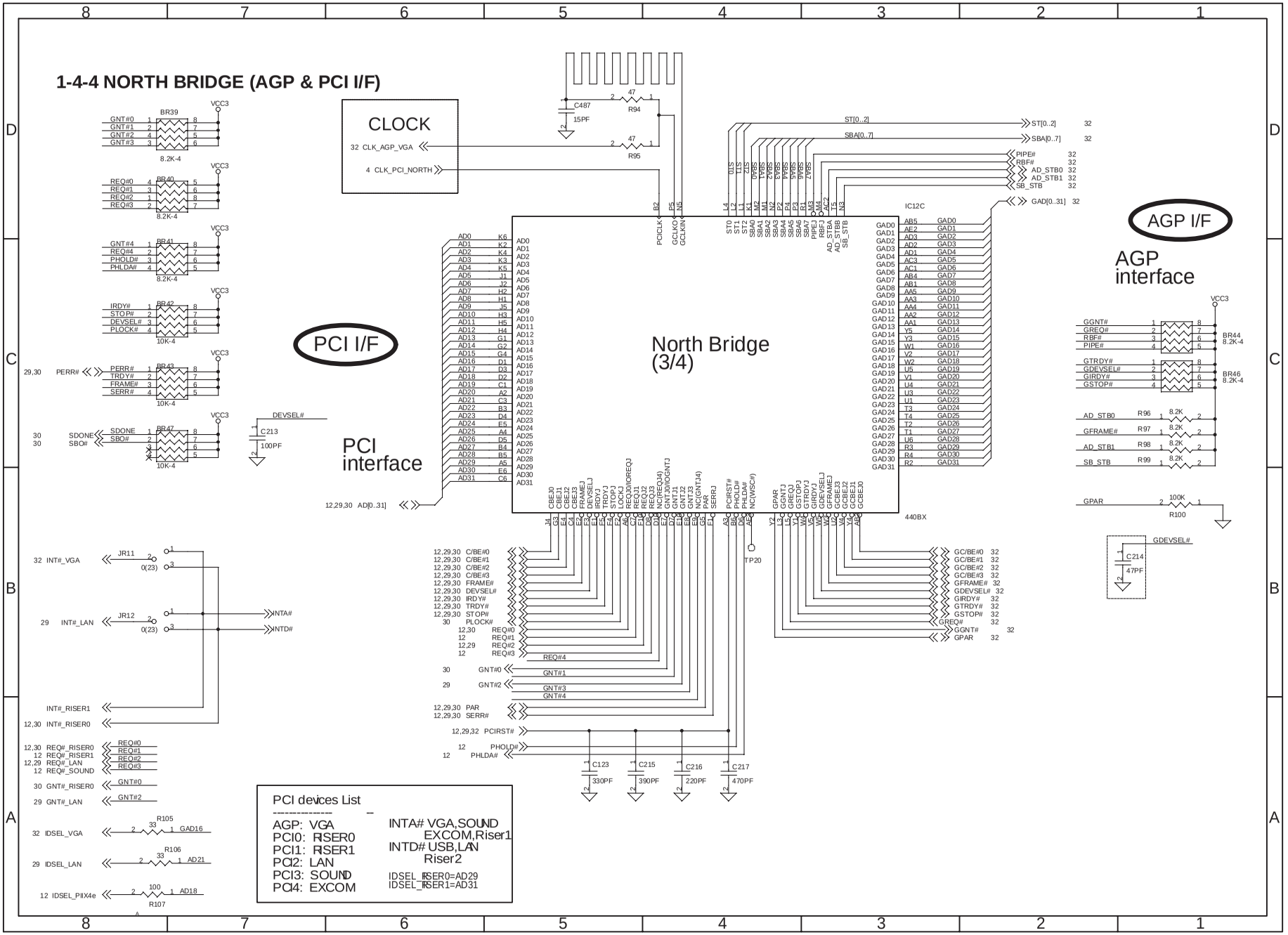

1-4-1 NORTH BRIDGE (CPU I/F)
HOST interface
HOST I/F
North Bridge (1/4)
CLOCK
HOST interface
GTL+ termination registors

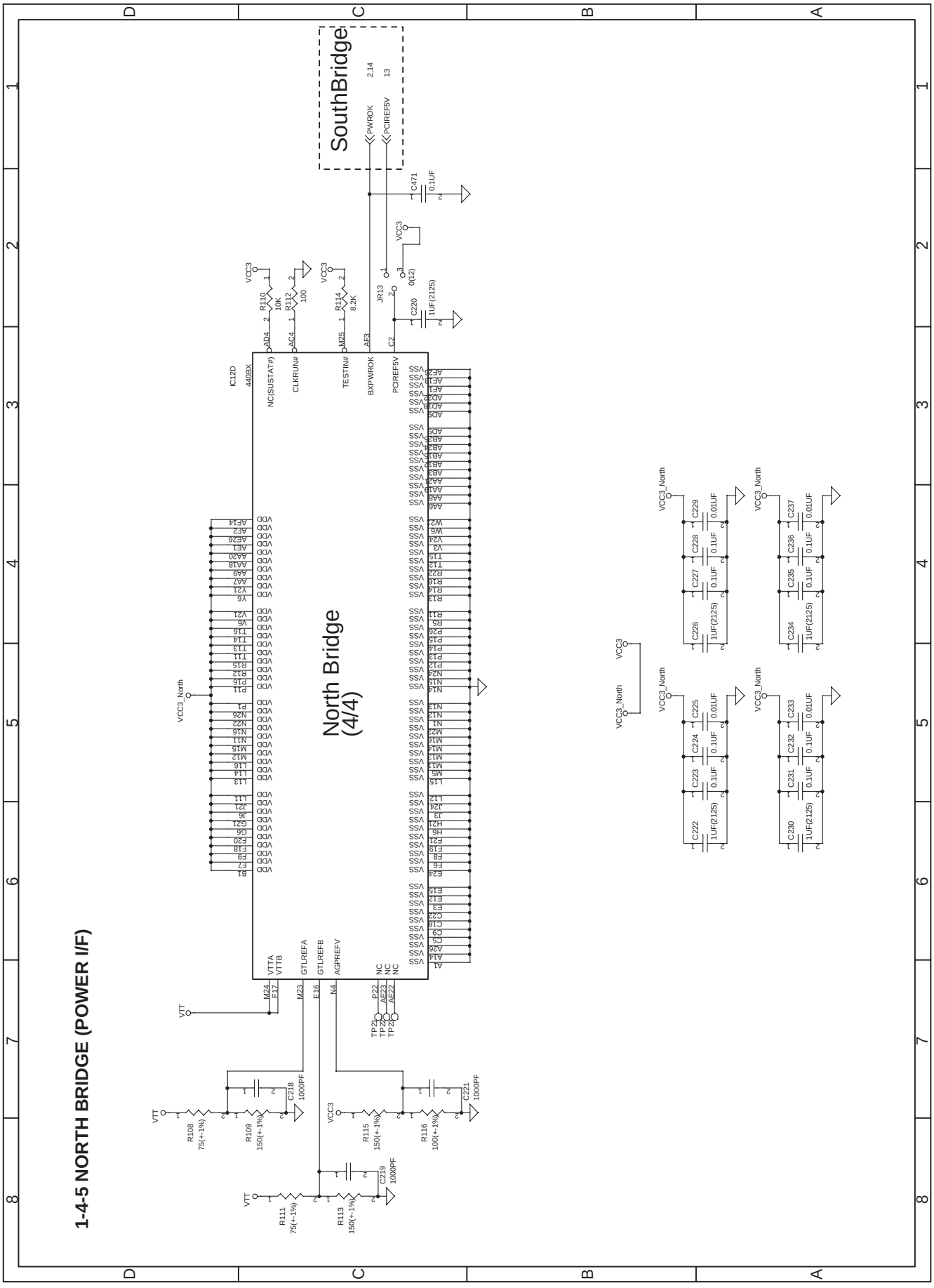

1-4-2 NORTH BRIDGE (SDRAM I/F)
DRAM I/F
SDRAM interface
MD[0..63]
MA[0..13]
CLK_SDRAM_BUFFERIN
CLK_SDRAM_FEEDBACK
CLOCK
North Bridge (2/4) SDRAM interface
IC12B
440BX
MECC[0..7]
SCS_A#[0..3]
SCS_B#[0..3]
SDQM[0..7]
SRAS#
SCAS#
MWE#
CLKEN[0..3]
HostBusBufferModeSelect
Pull-up: mobileLowPowerGTL+66MHz
Pull-down: desktopGTL+66MHzor100MHz
MemoryModuleConfig
Pull-up: 430-TX-compatible
Pull-down : normal-interface
AGP disable
Pull-up: disable
Pull-down: enable
QuickStartSelect
Pull-up: quick-start-mode
Pull-down: normal-stop-clock-mode
NorthBridge Hardware Configuration
QueueDepthEnable
Pull-up: pipelined-bus-mode
Pull-down: non-pipelined
HostFrequency select
Pull-up: 100MHz
Pull-down: 66MHz
CPU
100/66#

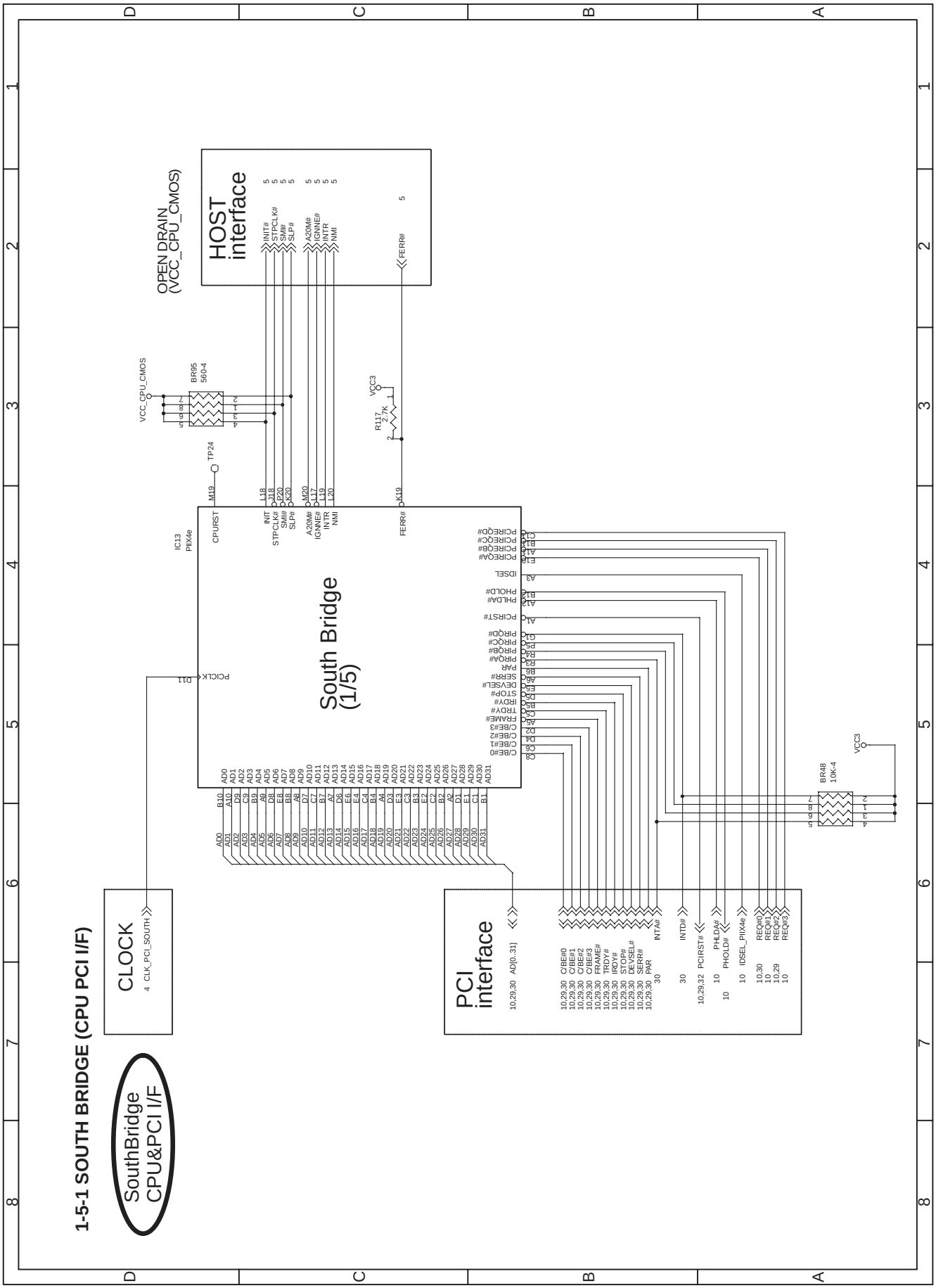
1-4-3 SDRAM (DIMM SOCKET)

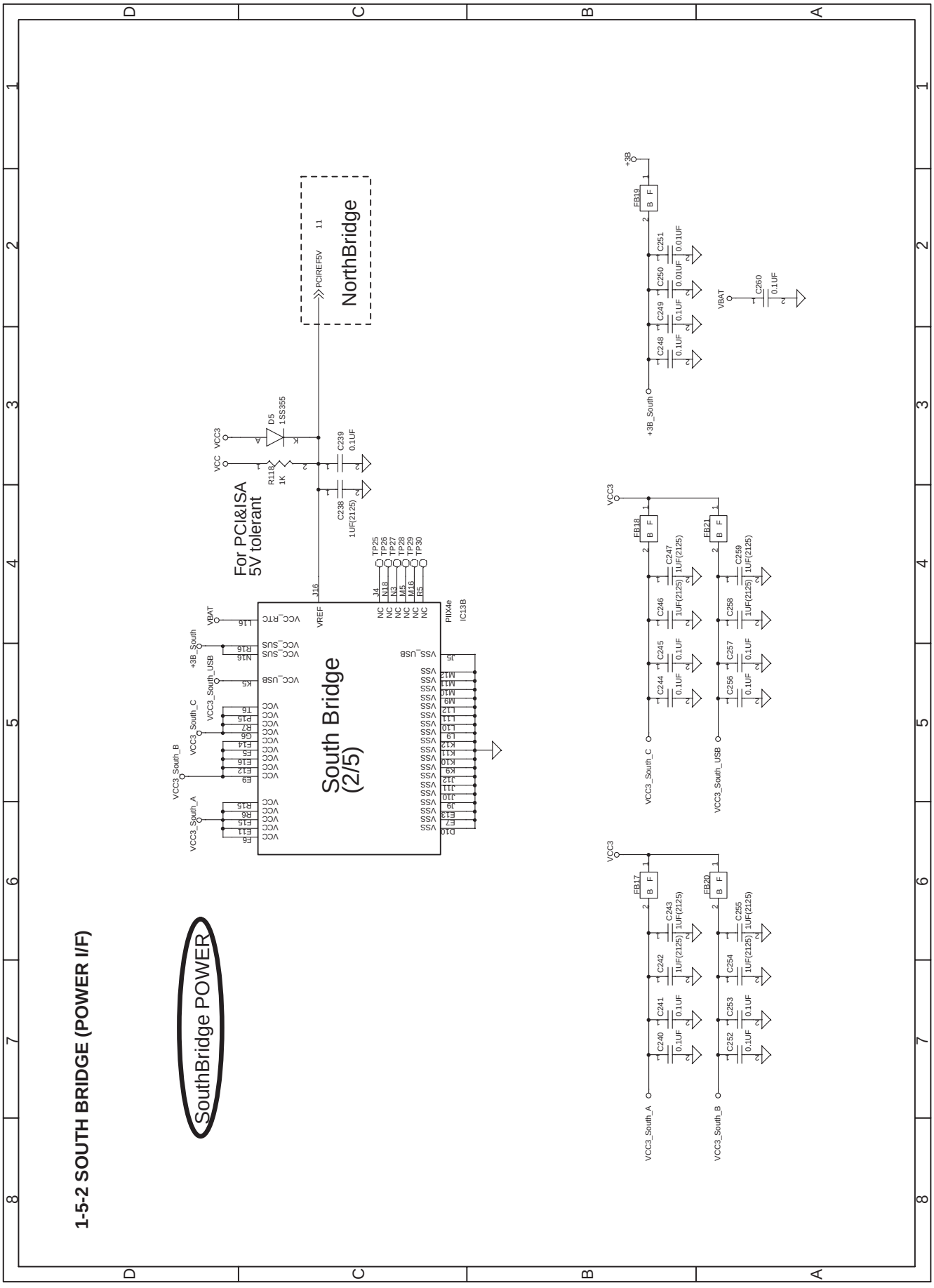


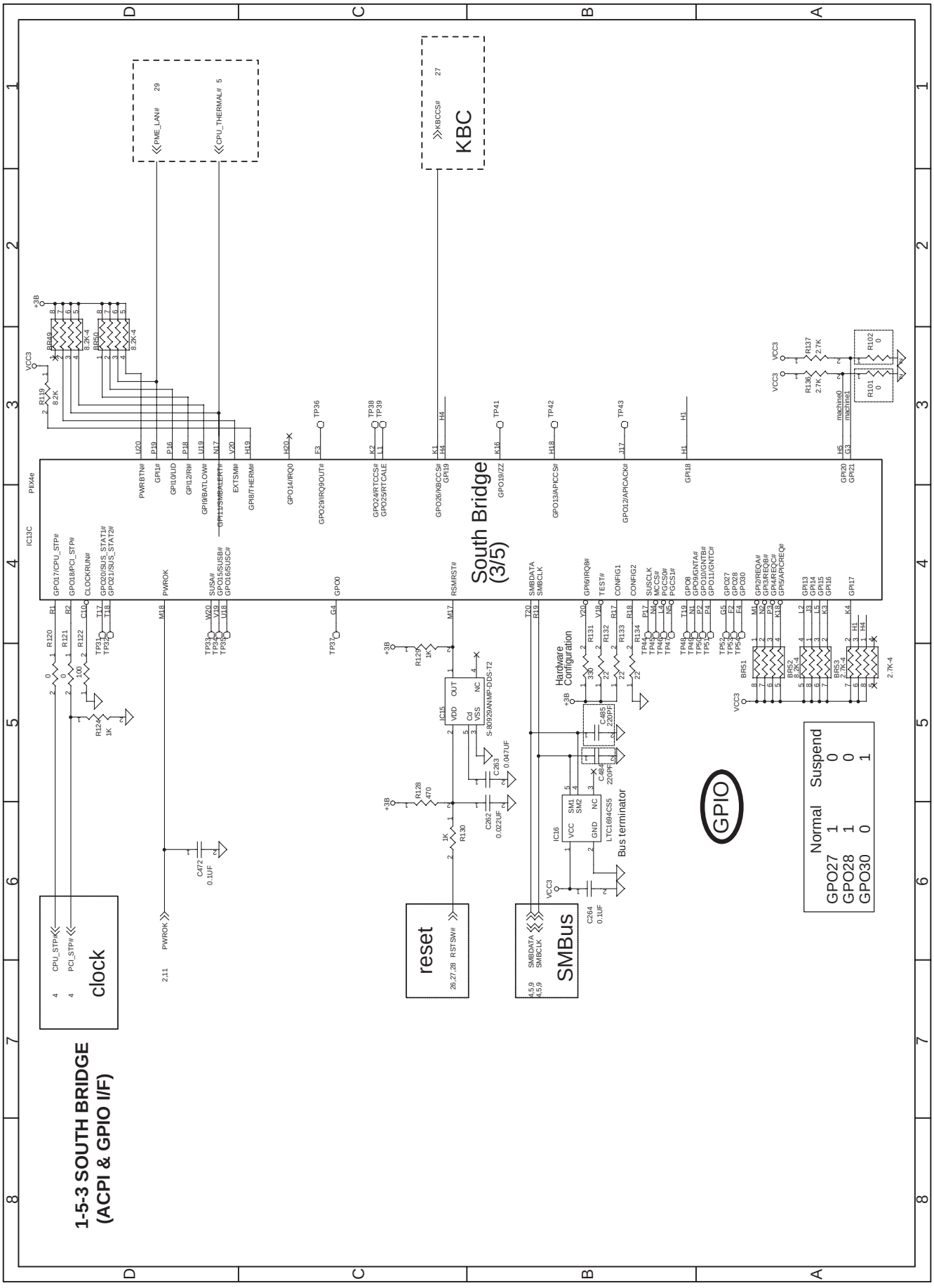
1-4-4 NORTH BRIDGE (AGP & PCI I/F)

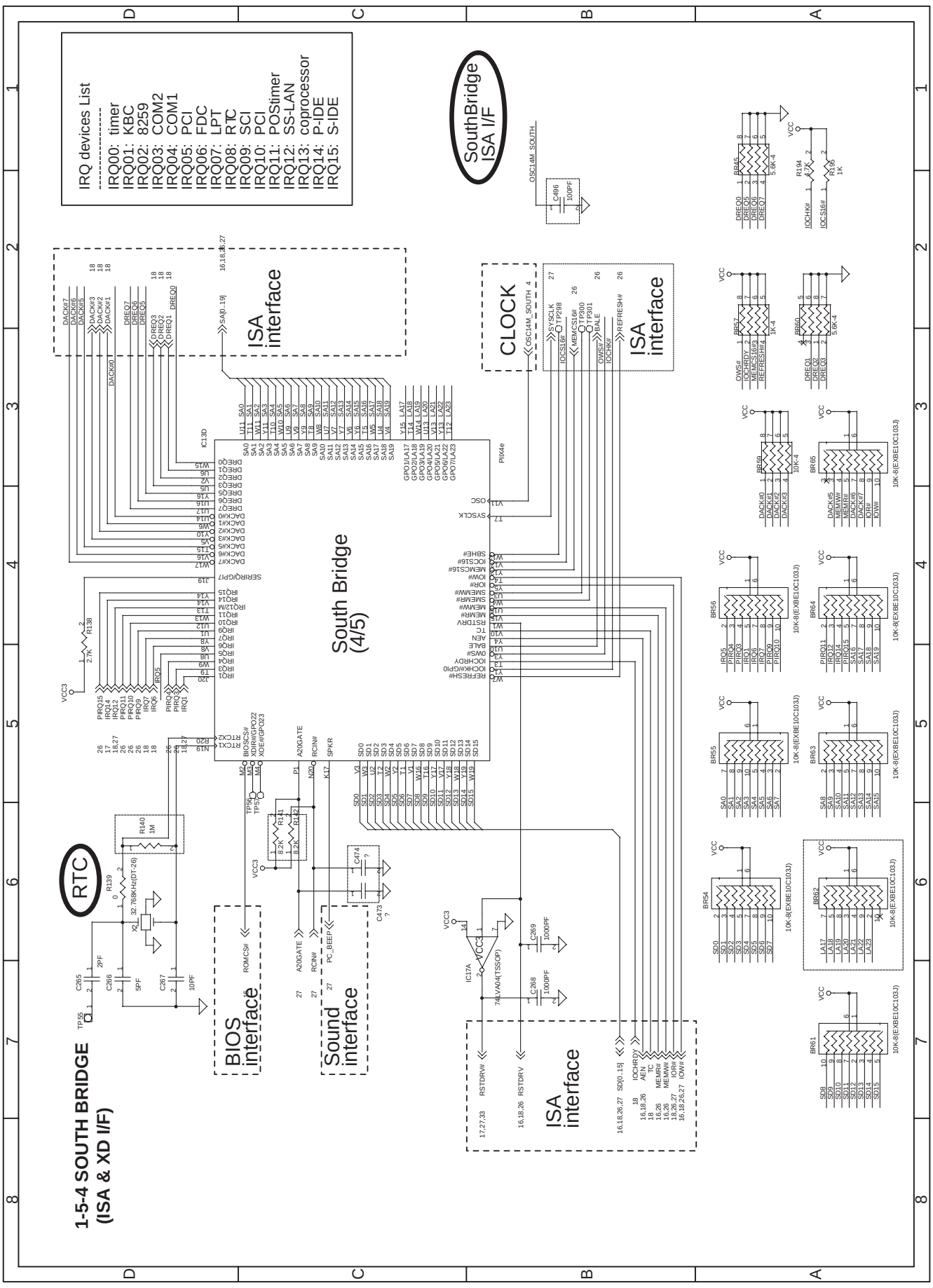


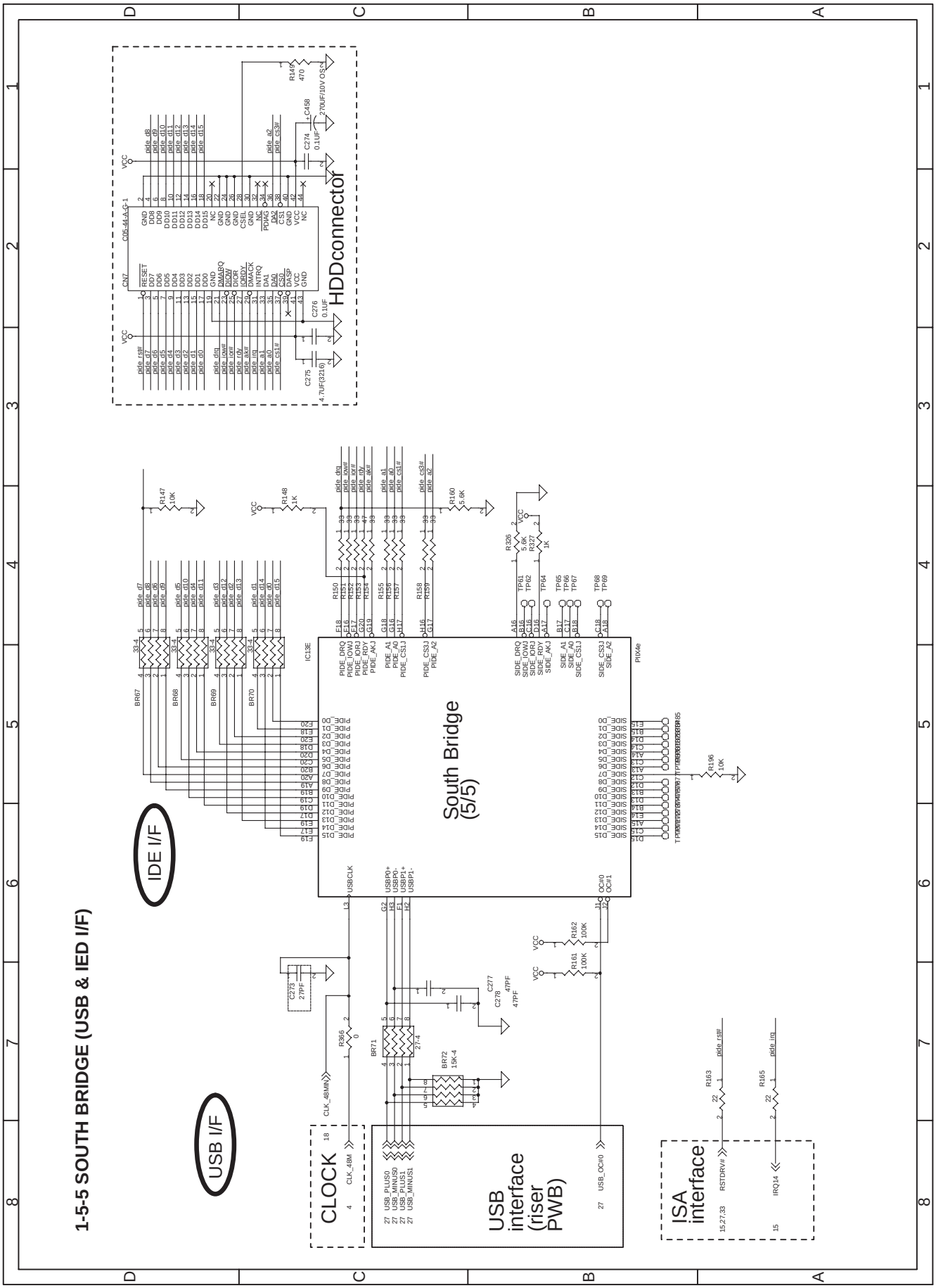

1-4-5 NORTH BRIDGE (POWER I/F)
North Bridge
(4/4)
SouthBridge
PWROK
PCIREF5V
IC12D
440BX
NC(SUSTAT#)
CLKRUN#
TESTIN#
BXPWROK
PCIREF5V
VTTA
VTTB
GTLREFA
GTLREFB
AGPREFV
NC
NC
NC
VCC3_North
VCC3
VTT
R108 75(+-1%)
R109 150(+-1%)
R111 75(+-1%)
R113 150(+-1%)
R115 150(+-1%)
R116 100(+-1%)
R110 10K
R112 100
R114 8.2K
C218 1000PF
C219 1000PF
C221 1000PF
C220 1UF(2125)
C471 0.1UF
JR13 0(12)
C222 1UF(2125)
C223 0.1UF
C224 0.1UF
C225 0.01UF
C226 1UF(2125)
C227 0.1UF
C228 0.1UF
C229 0.01UF
C230 1UF(2125)
C231 0.1UF
C232 0.1UF
C233 0.01UF
C234 1UF(2125)
C235 0.1UF
C236 0.1UF
C237 0.01UF


1-5-1 SOUTH BRIDGE (CPU PCI I/F)
SouthBridge
CPU&PCI I/F
CLOCK
4 CLK_PCI_SOUTH
PCI
interface
HOST
interface
OPEN DRAIN
(VCC_CPU_CMOS)
South Bridge
(1/5)
IC13
PIIX4e
CPURST
PCICLK
VCC_CPU_CMOS
BR95
560-4
TP24
R117
2.7K
VCC3
BR48
10K-4
INIT#
STPCLK#
SMI#
SLP#
A20M#
IGNNE#
INTR
NMI
FERR#
IDSEL
PHLDA#
PHOLD#
PCIRST#
PIRQD#
PIRQC#
PIRQB#
PIRQA#
PAR
SERR#
DEVSEL#
STOP#
IRDY#
TRDY#
FRAME#
C/BE#3
C/BE#2
C/BE#1
C/BE#0
AD[0..31]
INTD#
PCIRST#
PHLDA#
PHOLD#
IDSEL_PIIX4e
REQ#0
REQ#1
REQ#2
REQ#3


1-5-2 SOUTH BRIDGE (POWER I/F)
SouthBridge POWER
South Bridge
(2/5)
PIX4e
IC13B
NorthBridge
PCIREF5V
For PCI&ISA
5V tolerant
VCC3
VCC
VBAT
+3B
+3B_South
VCC3_South_A
VCC3_South_B
VCC3_South_C
VCC3_South_USB
VCC3_South_South_USB
R118
1K
D5
1SS355
C239
0.1UF
C238
1UF(2125)
C260
0.1UF
C240
C241
C242
C243
C244
C245
C246
C247
C248
C249
C250
C251
C252
C253
C254
C255
C256
C257
C258
C259
0.1UF
1UF(2125)
0.01UF
FB17
FB18
FB19
FB20
FB21
TP25
TP26
TP27
TP28
TP29
TP30


1-5-3 SOUTH BRIDGE
(ACPI & GPIO I/F)
South Bridge
(3/5)
PIIX4e
IC13C
KBC
clock
reset
SMBus
GPIO
Hardware
Configuration
Bus terminator
Normal Suspend
GPO27 1 0
GPO28 1 0
GPO30 0 1


1-5-4 SOUTH BRIDGE
(ISA & XD I/F)
IRQ devices List
IRQ00: timer
IRQ01: KBC
IRQ02: 8259
IRQ03: COM2
IRQ04: COM1
IRQ05: PCI
IRQ06: FDC
IRQ07: LPT
IRQ08: RTC
IRQ09: SCI
IRQ10: PCI
IRQ11: POStimer
IRQ12: SS-LAN
IRQ13: coprocessor
IRQ14: P-IDE
IRQ15: S-IDE
SouthBridge
ISA I/F
ISA interface
CLOCK
ISA interface
South Bridge
(4/5)
RTC
BIOS interface
Sound interface
ISA interface
IC13D
PIIX4e
IC17A
74LV04(TSSOP)
OSC14M_SOUTH
SYSCLK
IOCS16#
MEMCS16#
OWS#
IOCHK#
REFRESH#
BALE
SERIRQ/GPI7
ROMCS#
PC_BEEP
A20GATE
RCIN#
SPKR
RSTDRV#
RSTDRV
IOCHRDY
AEN
TC
MEMR#
MEMW#
IOR#
IOW#
SD[0..15]
SA[0..19]
LA[17..23]
DACK#[0..7]
DREQ[0..7]
IRQ[1,3..15]
SERIRQ/GPI7
SMIACT#/GPO22
XOE#/GPO23
SMI#/GPO27
SUSA#/GPO20
SUSB#/GPO21
SUSC#/GPO17
SLP_S3#/GPO18
SLP_S5#/GPO19
PWROK/GPO16
PCIRST#/GPO32
GPO1/LA17
GPO2/LA18
GPO3/LA19
GPO4/LA20
GPO5/LA21
GPO6/LA22
GPO7/LA23
SBHE#
MEMCS16#
IOCS16#
IOW#
IOR#
SMEMW#
SMEMR#
MEMW#
MEMR#
RSTDRV
TC
AEN
BALE
IOCHRDY
IOCHK#/GPI0
REFRESH#
OSC
SYSCLK
R138 2.7K
R140 1M
R139 0
X2 32.768KHz(DT-26)
C265 2PF
C266 5PF
C267 10PF
R141 8.2K
R142 8.2K
C474 ?
C473 ?
C269 1000PF
C268 1000PF
C496 100PF
R194 1K
R195 1K
BR45 5.6K-4
BR57 1K-4
BR60 5.6K-4
BR59 10K-4
BR56 10K-8(EXBE10C103J)
BR64 10K-8(EXBE10C103J)
BR55 10K-8(EXBE10C103J)
BR63 10K-8(EXBE10C103J)
BR54 10K-8(EXBE10C103J)
BR62 10K-8(EXBE10C103J)
BR61 10K-8(EXBE10C103J)
BR65 10K-8(EXBE10C103J)


1-5-5 SOUTH BRIDGE (USB & IED I/F)
IDE I/F
USB I/F
South Bridge (5/5)
IC13E
PIXI4E
HDDconnector
CN7
C06-44A-G-1
USB interface (riser PWB)
CLOCK
ISA interface
USB_PLUS0
USB_MINUS0
USB_PLUS1
USB_MINUS1
CLK_48MIN
CLK_48M
USB_OC#0
RSTDRV#
IRQ14
pide_rst#
pide_irq
VCC
R147 10K
R148 1K
R149 470
R160 5.6K
R326 5.6K
R327 1K
R196 10K
R161 100K
R162 100K
R163 22
R165 22
R366 0
C273 27PF
C274 0.1UF
C275 4.7UF(3216)
C276 0.1UF
C277 47PF
C278 47PF
C458 270UF/10V OSCN
BR67
BR68
BR69
BR70
BR71 27-4
BR72 15K-4
R150
R152
R153
R154
R155
R156
R157
R158
R159
TP61
TP62
TP64
TP65
TP66
TP67
TP68
TP69

1-6 BIOS

BIOS

ISA interface

15,18,26,27 SA[0..19]
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16 SA17 SA18 SA19

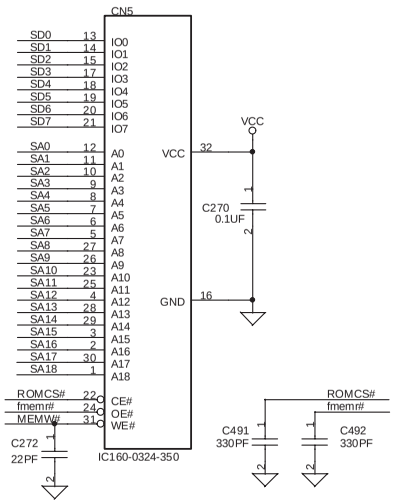
15,18,26,27 SD[0..15]
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7

15,18,26 RSTDRV
15,18,26,27 IOR#
15,18,26,27 IOW#
15,18,26 AEN
15,26 MEMW#
15,26 MEMR#

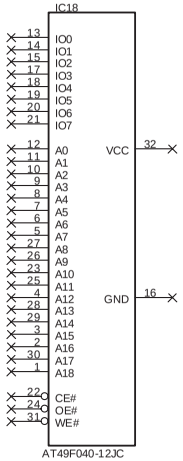
BIOS interface

15 ROMCS#

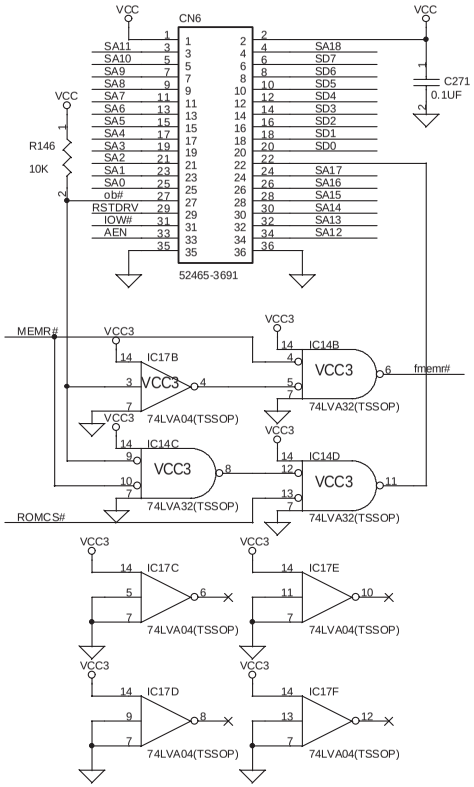
FLASH socket

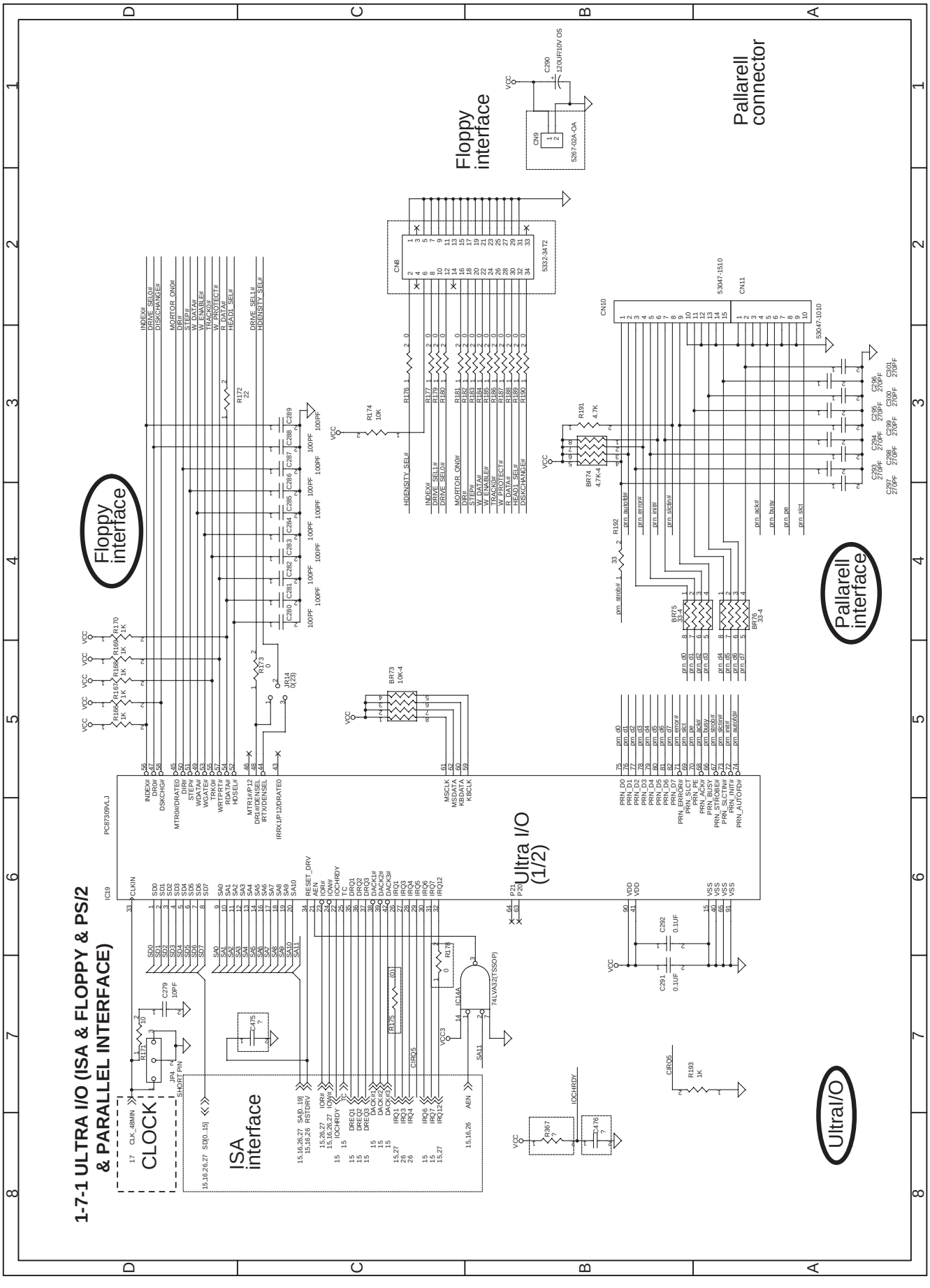


FLASH ROM

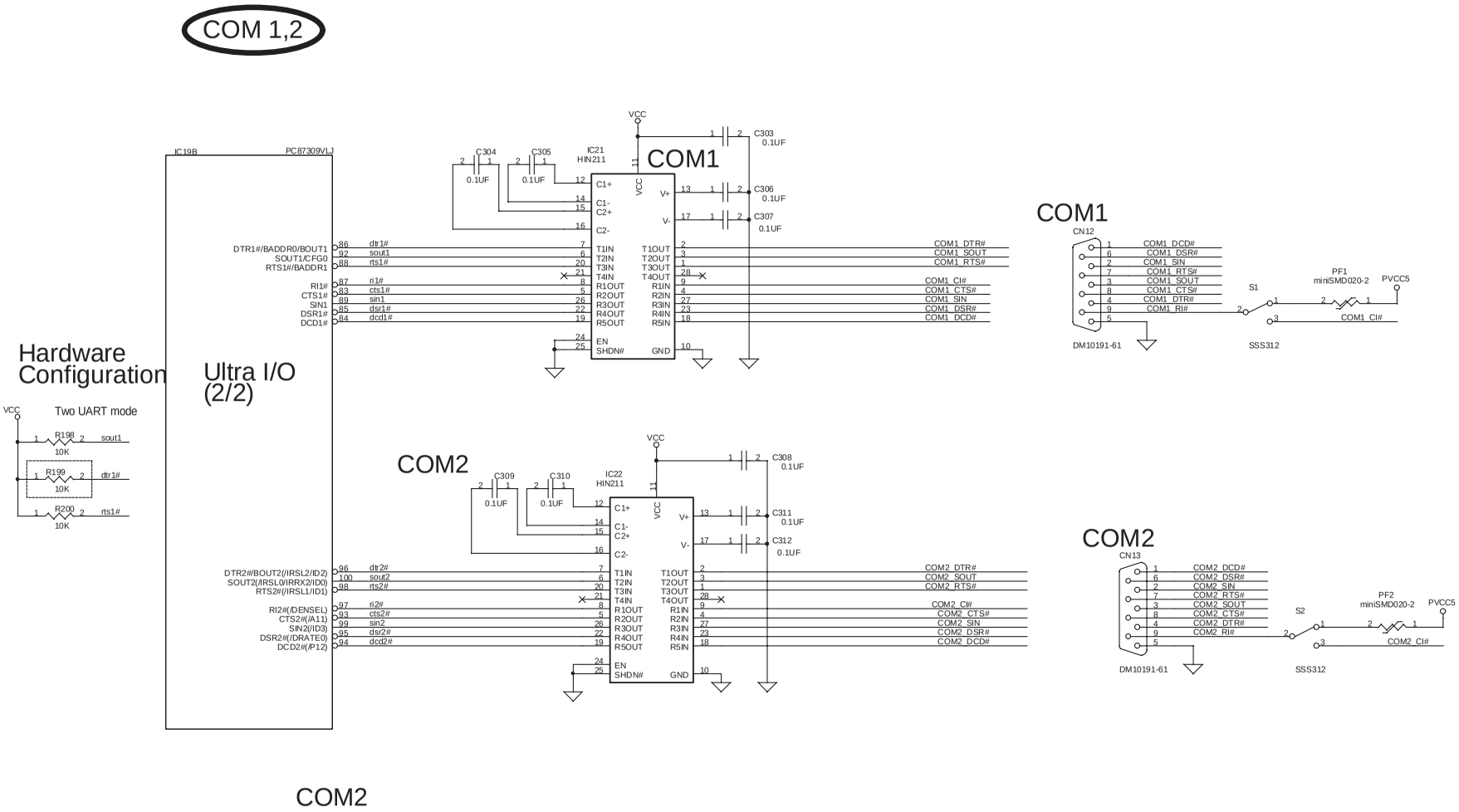


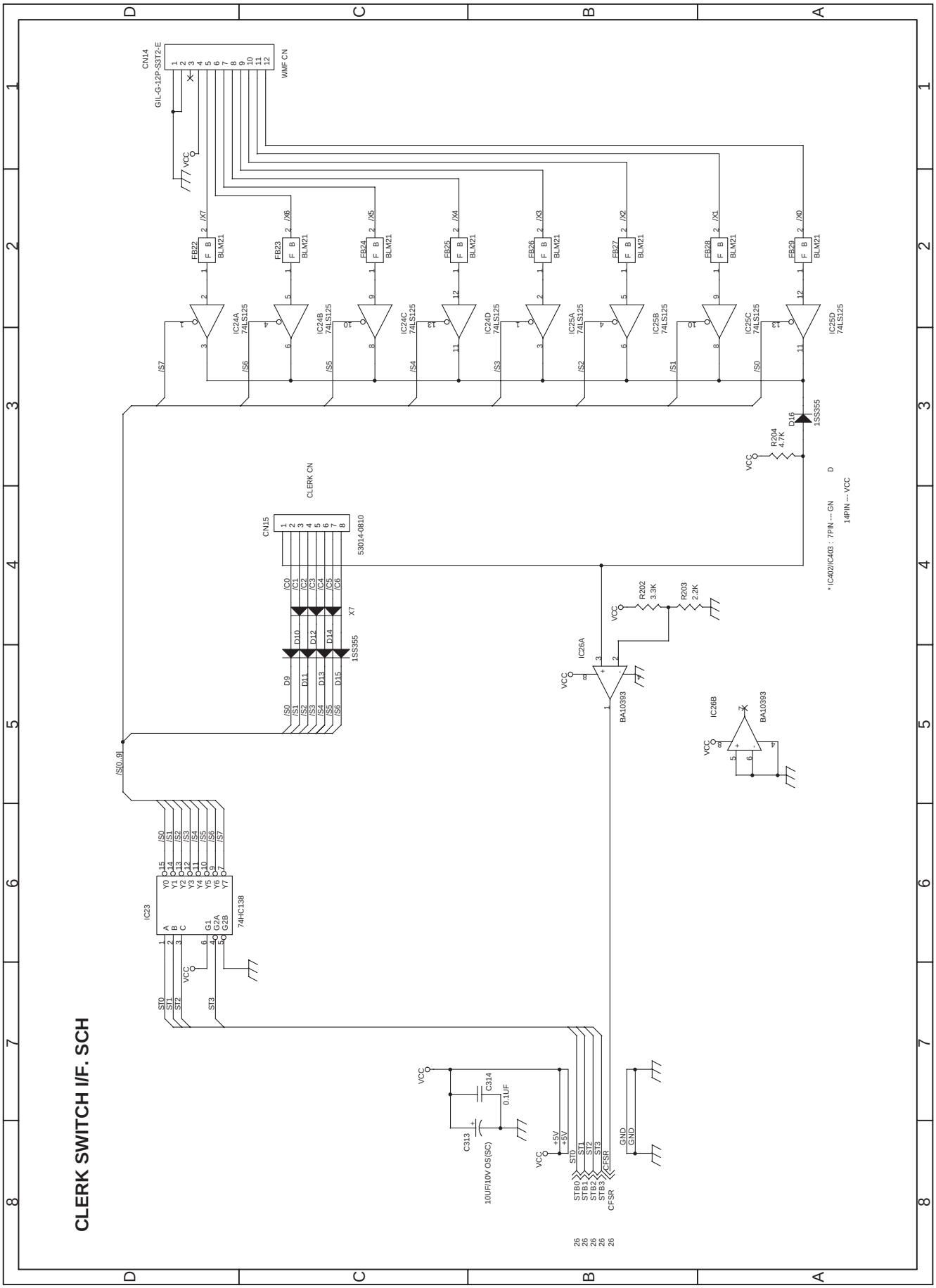
HelpBoard

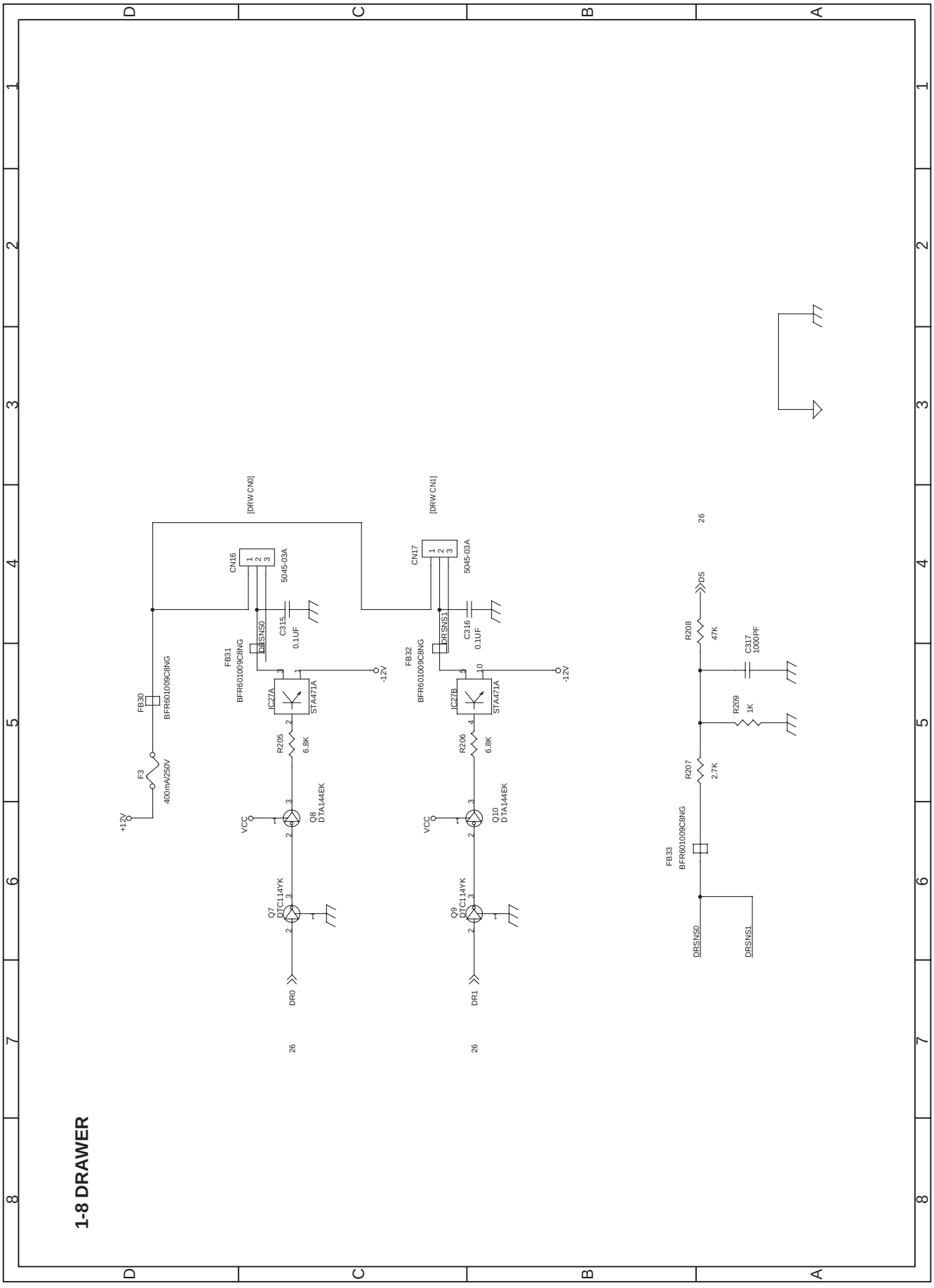



1-7-1 ULTRA I/O (ISA & FLOPPY & PS/2 & PARALLEL INTERFACE)
CLOCK
ISA interface
Ultra I/O (1/2)
Floppy interface
Floppy interface
Pallarell connector
Pallarell interface
Ultral/O

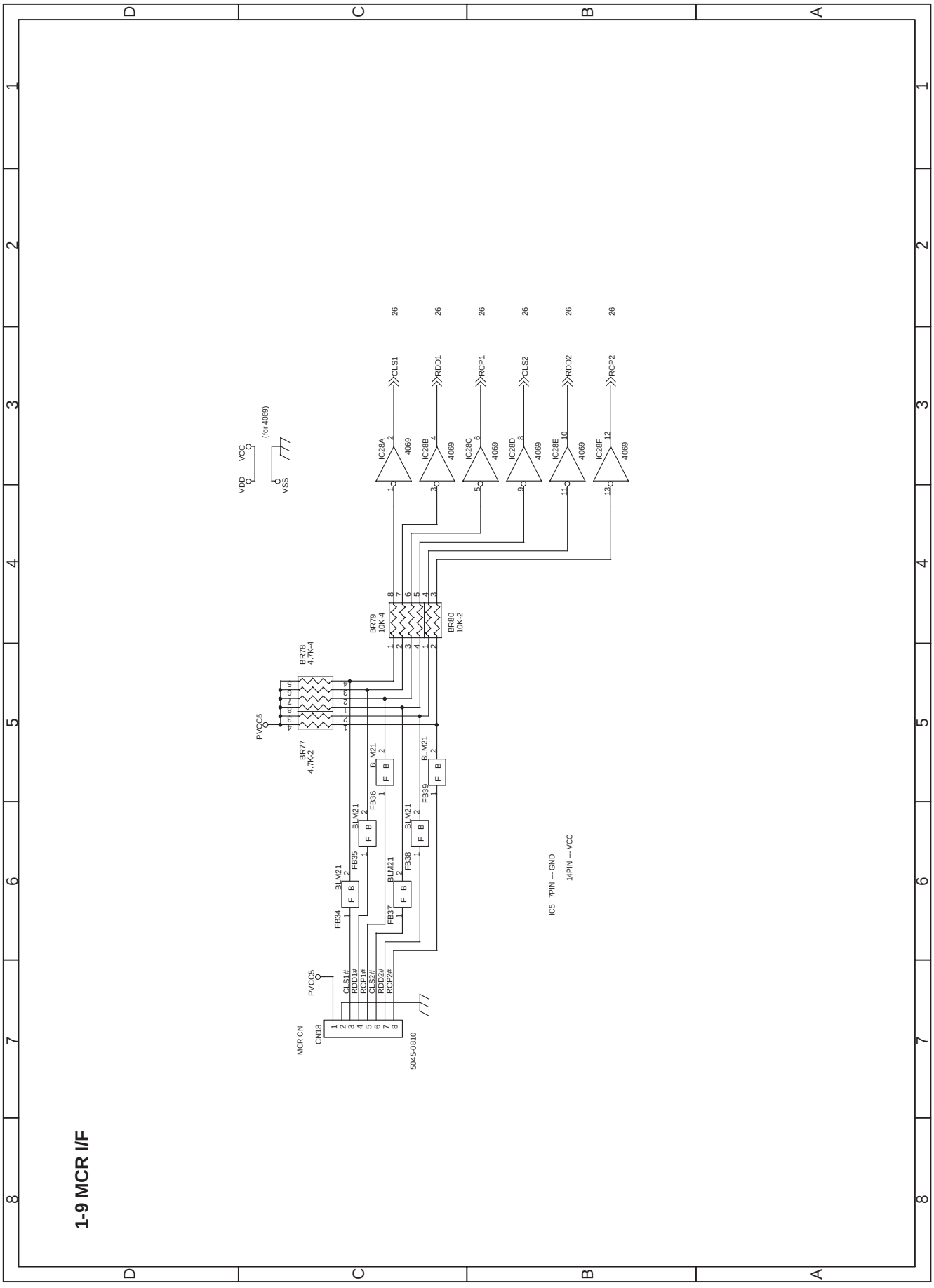
1-7-2 ULTRA I/O COMx2

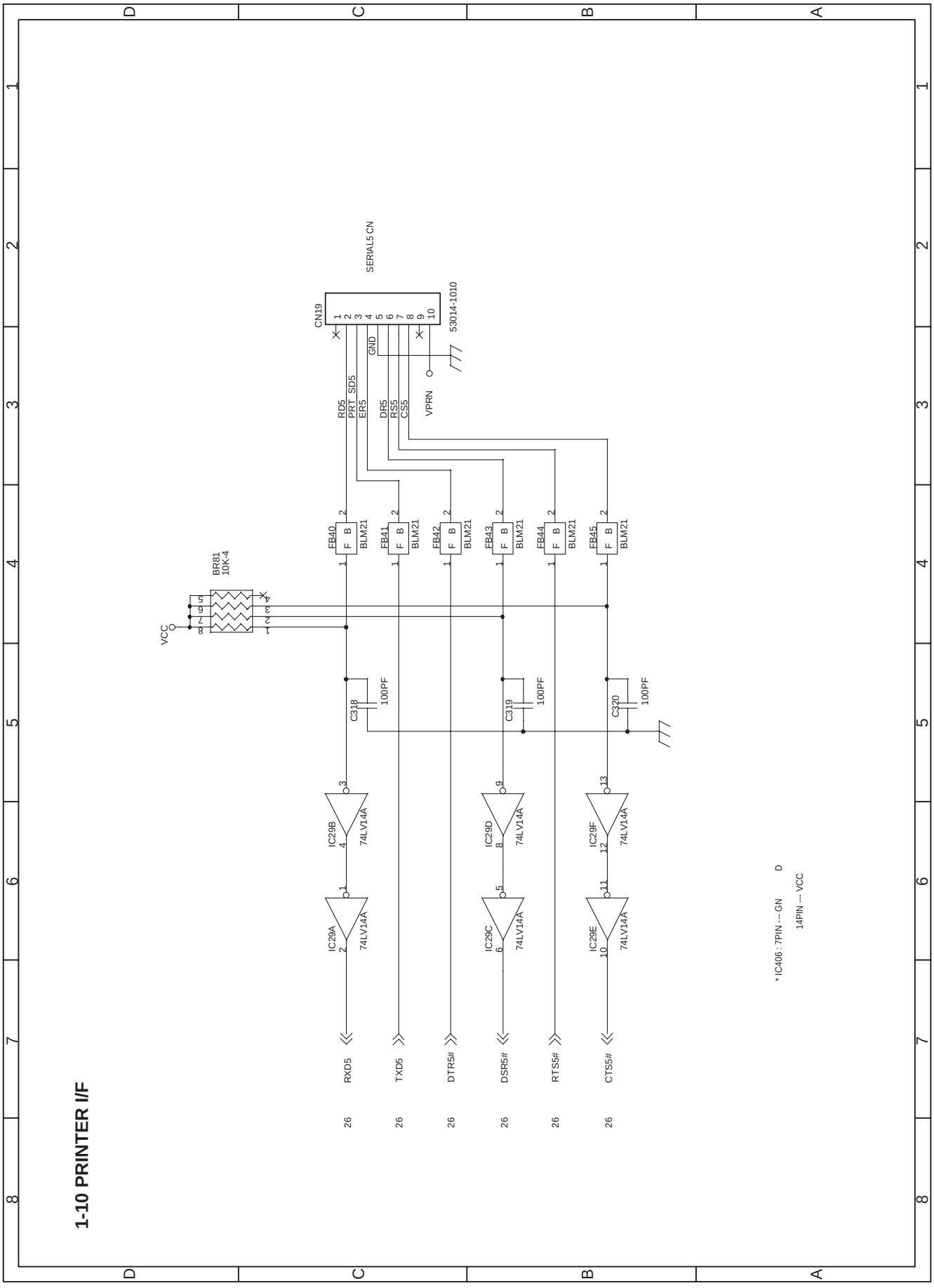


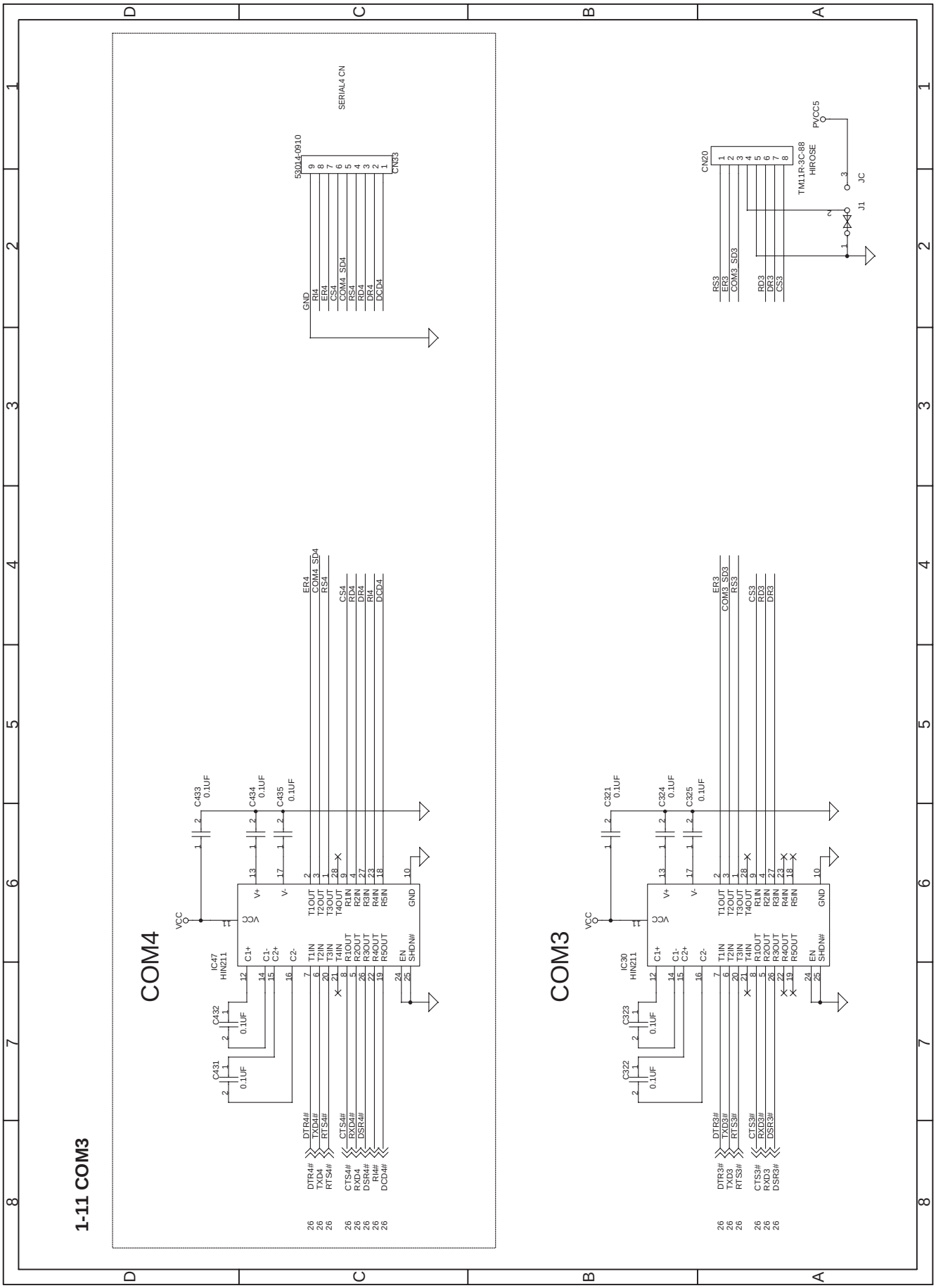

CLERK SWITCH I/F. SCH
CN14
GIL-G-12P-S3T2-E
WMF CN
CN15
53014-0810
CLERK CN
IC23
74HC138
IC24A 74LS125
IC24B 74LS125
IC24C 74LS125
IC24D 74LS125
IC25A 74LS125
IC25B 74LS125
IC25C 74LS125
IC25D 74LS125
IC26A
IC26B
BA10393
FB22 BLM21
FB23 BLM21
FB24 BLM21
FB25 BLM21
FB26 BLM21
FB27 BLM21
FB28 BLM21
FB29 BLM21
D16 1SS355
D9 D10 D11 D12 D13 D14 D15 1SS355
R204 4.7K
R202 3.3K
R203 2.2K
C313 10UF/10V OS(SC)
C314 0.1UF
VCC
GND
+5V
/S0_9
* IC402/IC403 : 7PIN --- GN 14PIN --- VCC

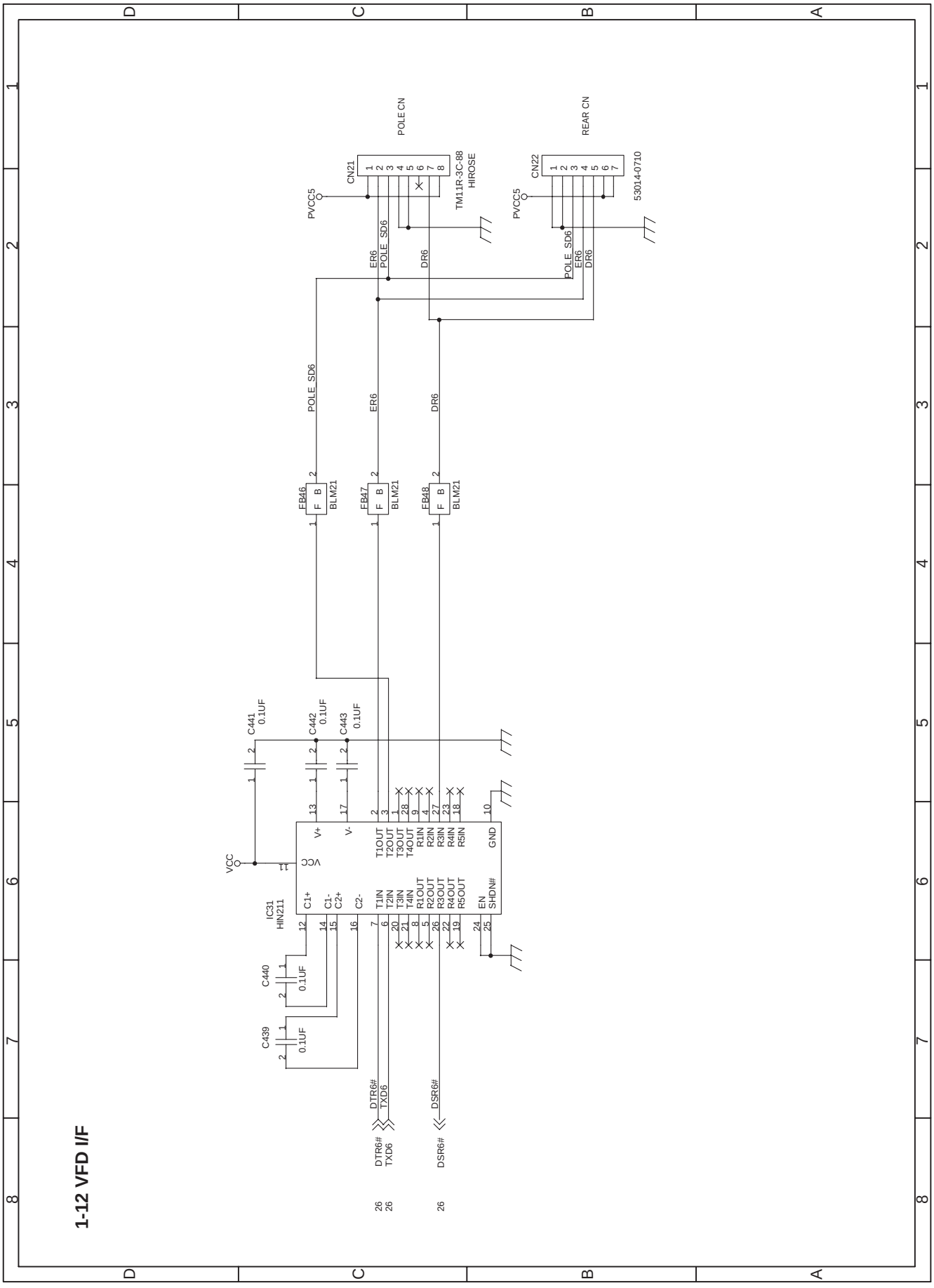

1-8 DRAWER
[DRW CN0]
[DRW CN1]
CN16
CN17
5045-03A
C315
0.1UF
C316
0.1UF
FB31
FB32
FB33
FB30
BFR601009C8NG
DRSNS0
DRSNS1
IC27A
IC27B
STA471A
R205
R206
6.8K
R207
2.7K
R208
47K
R209
1K
C317
1000PF
Q7
Q9
DTC114YK
Q8
Q10
DTA144EK
VCC
+12V
-12V
F3
400mA/250V
DR0
DR1
DS
26

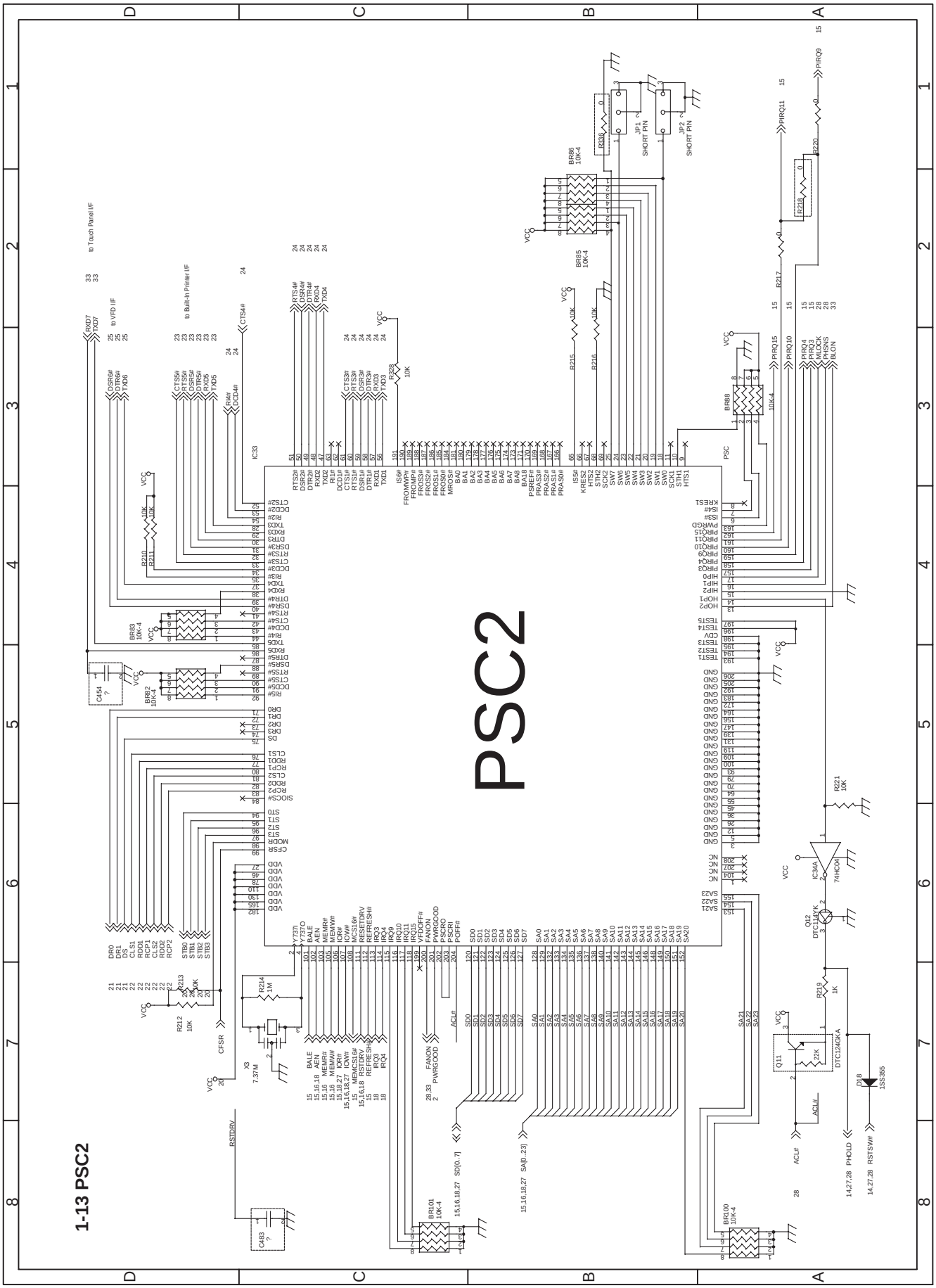
1-9 MCR I/F

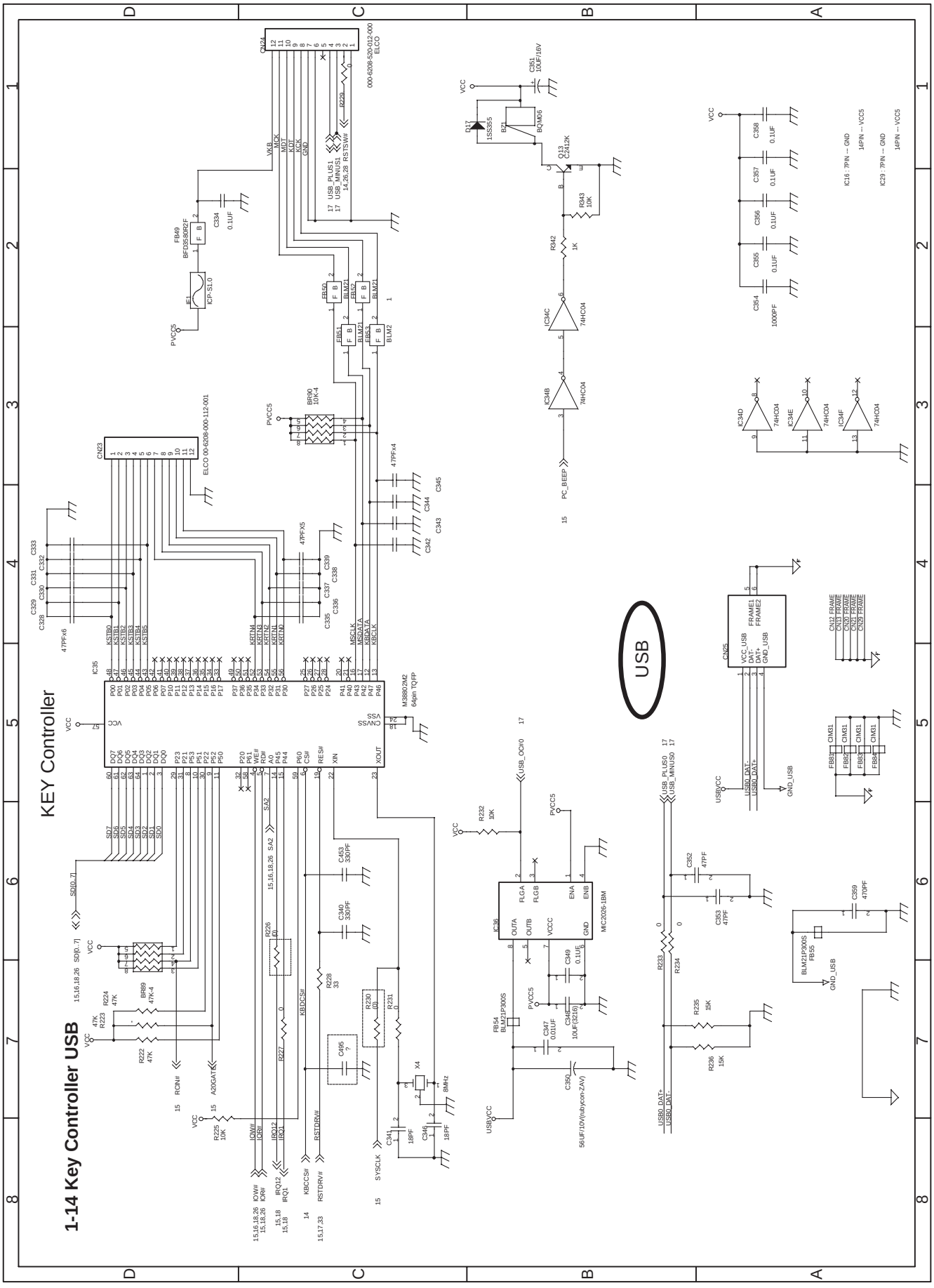

CLS1
RDD1
RCP1
CLS2
RDD2
RCP2
IC28A
IC28B
IC28C
IC28D
IC28E
IC28F
4069
VDD
VCC
VSS
(for 4069)
BR79
10K-4
BR80
10K-2
BR78
4.7K-4
BR77
4.7K-2
PVCC5
BLM21
FB34
FB35
FB36
FB37
FB38
FB39
CLS1#
RDD1#
RCP1#
CLS2#
RDD2#
RCP2#
MCR CN
CN18
5045-0810
IC5 : 7PIN --- GND
14PIN --- VCC

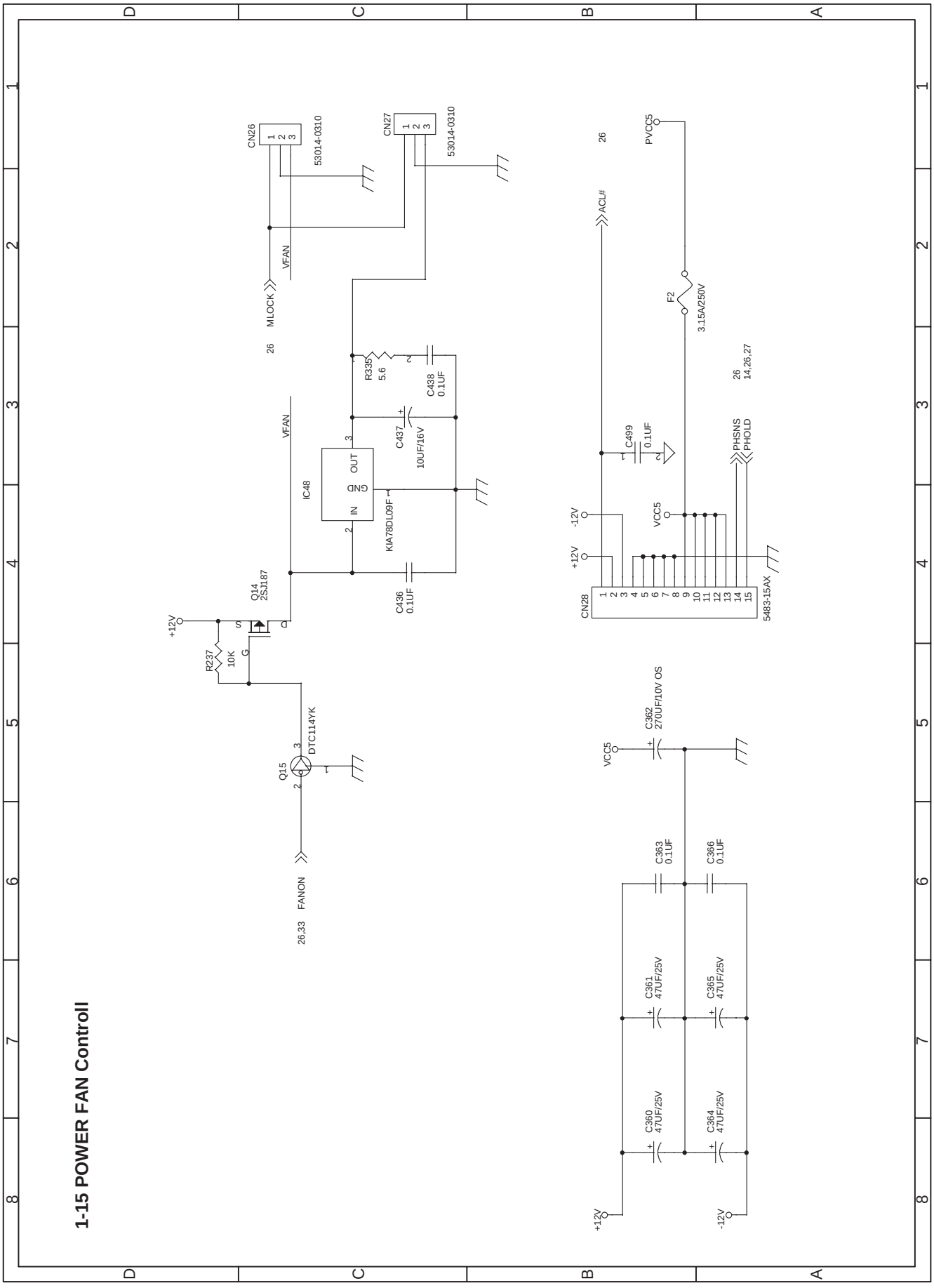

1-10 PRINTER I/F
SERIAL5 CN
CN19
53014-1010
GND
VPRN
RD5
PRT SD5
ER5
DR5
RS5
CS5
BR81
10K-4
VCC
FB40
FB41
FB42
FB43
FB44
FB45
BLM21
C318
C319
C320
100PF
IC29A
IC29B
IC29C
IC29D
IC29E
IC29F
74LV14A
RXD5
TXD5
DTR5#
DSR5#
RTS5#
CTS5#
26
* IC406 : 7PIN --- GN D
14PIN --- VCC

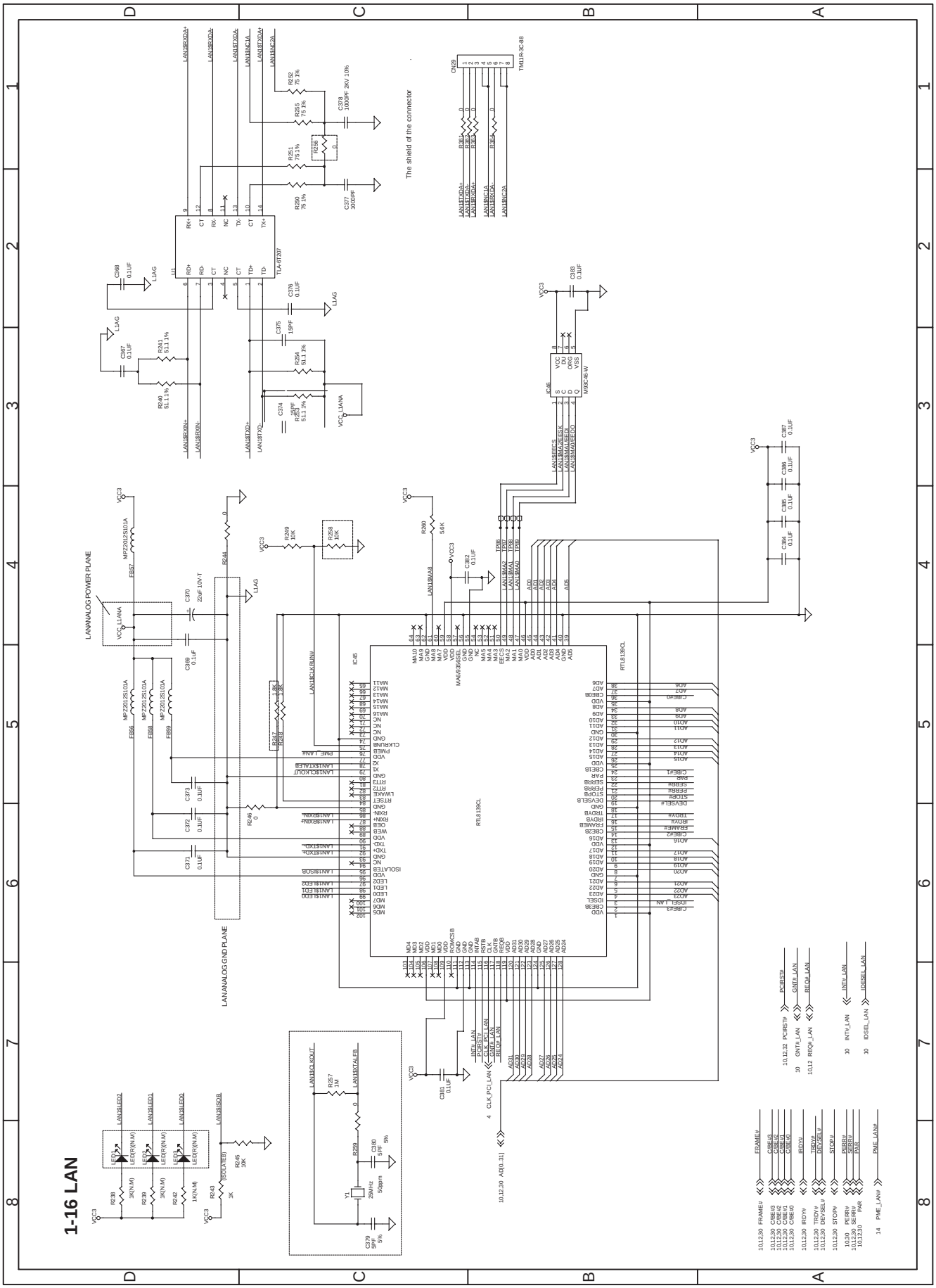

1-11 COM3
COM4
COM3
SERIAL4 CN
CN33
53014-0910
GND
R4
ER4
CS4
COM4_SD4
RS4
RD4
DR4
DCD4
CN20
TM11R-3C-88
HIROSE
PVCC5
JC
J1
RS3
ER3
COM3_SD3
RD3
DR3
CS3
IC47
IC30
HIN211
VCC
C+
V+
V-
C1+
C1-
C2+
C2-
T1IN
T2IN
T3IN
T4IN
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
T1OUT
T2OUT
T3OUT
T4OUT
R1IN
R2IN
R3IN
R4IN
R5IN
EN
SHDN#
GND
C431
C432
C433
C434
C435
C321
C322
C323
C324
C325
0.1UF
DTR4#
TXD4
RTS4#
CTS4#
RXD4
DSR4#
RI4#
DCD4#
DTR3#
TXD3
RTS3#
CTS3#
RXD3
DSR3#

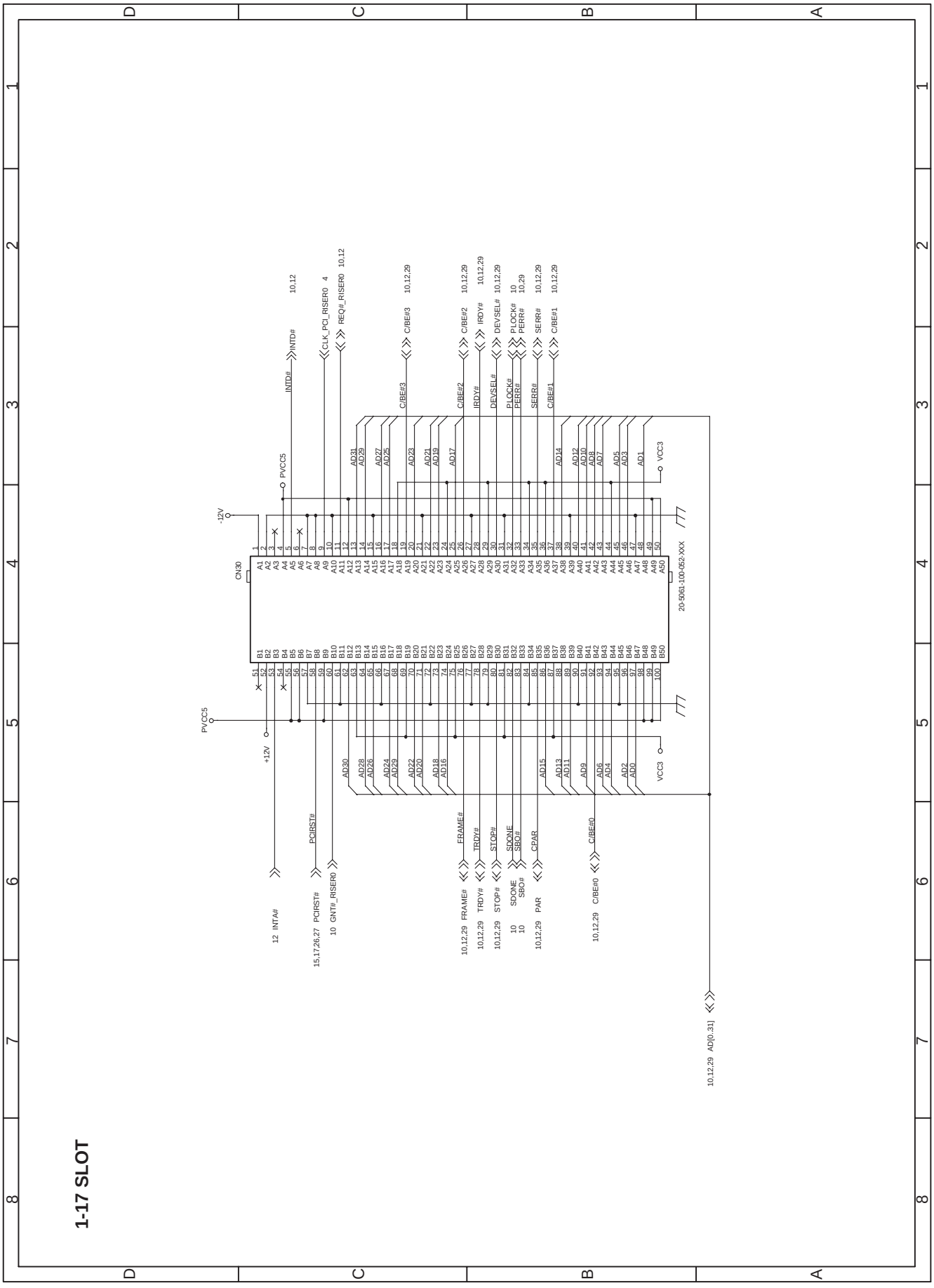

1-12 VFD I/F
POLE CN
REAR CN
CN21
CN22
TM11R-3C-88
HIROSE
53014-0710
PVCC5
POLE_SD6
ER6
DR6
FB46
FB47
FB48
BLM21
C441
C442
C443
C439
C440
0.1UF
IC31
HIN211
VCC
V+
V-
C1+
C1-
C2+
C2-
T1OUT
T2OUT
T3OUT
T4OUT
R1IN
R2IN
R3IN
R4IN
R5IN
GND
T1IN
T2IN
T3IN
T4IN
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
EN
SHDN#
DTR6#
TXD6
DSR6#

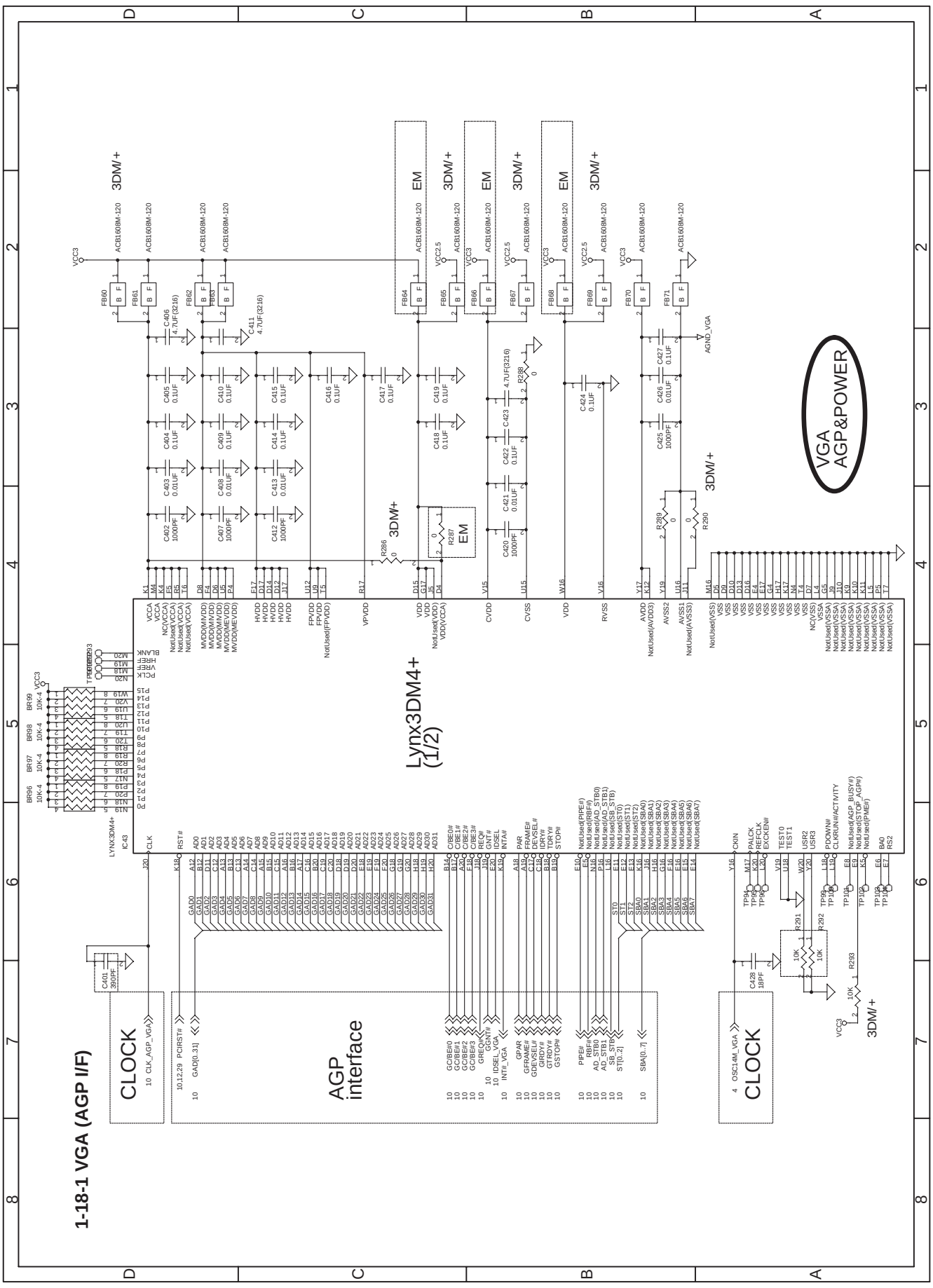

PSC2
1-13 PSC2

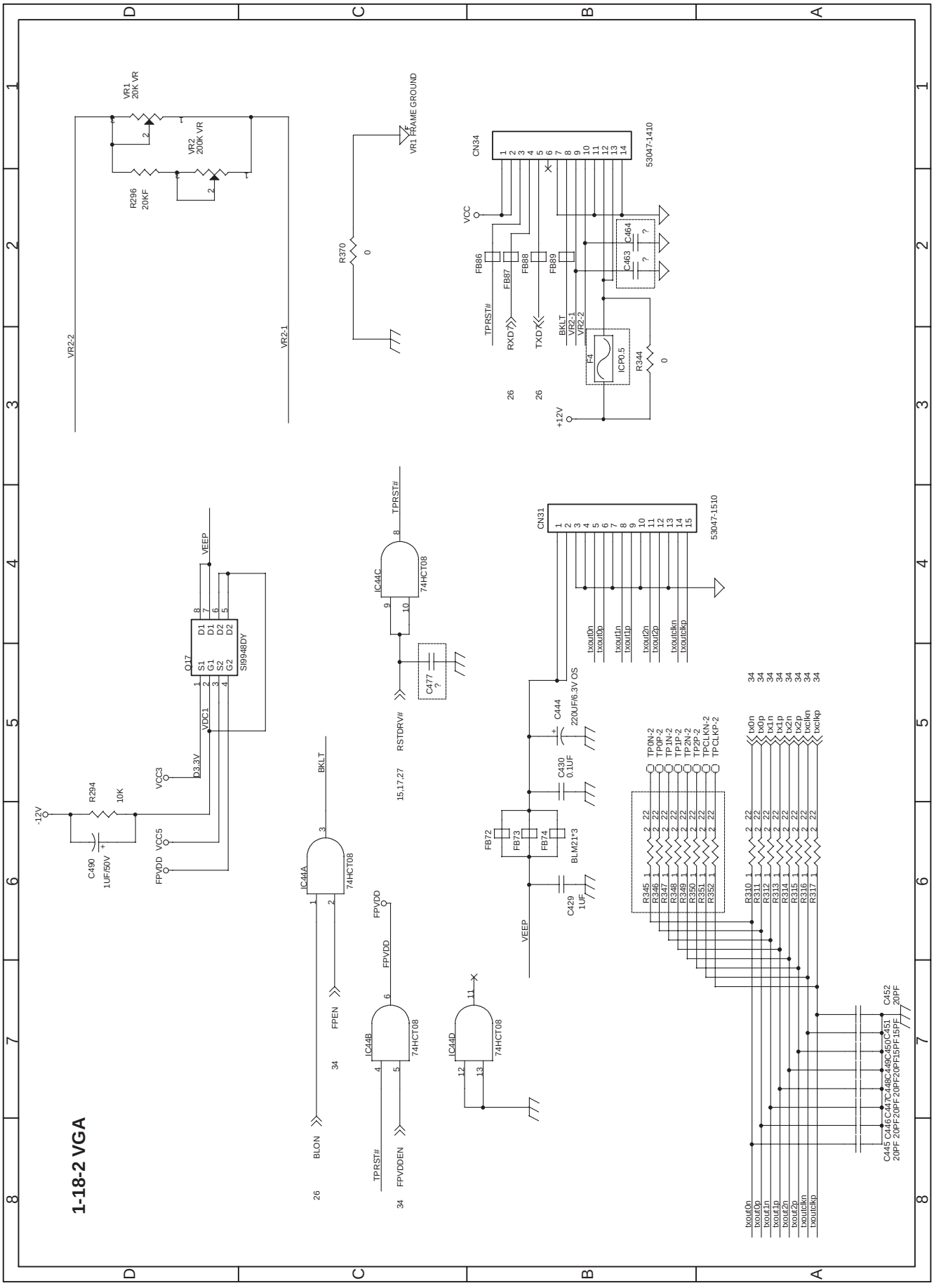

1-14 Key Controller USB
KEY Controller
USB
IC35
M38802M2
64pin TQFP
IC36
MIC2026-1BM
CN23
ELCO 00-6208-000-112-001
CN24
000-6208-520-012-000
ELCO
CN25
VCC_USB
DAT-
DAT+
GND_USB
FRAME1
FRAME2
IC1
ICP-S1.0
D17
1SS355
Q13
2SK12K
IC34A
IC34B
IC34C
IC34D
IC34E
IC34F
74HC04
BR89
47K-4
BR90
10K-4
X4
8MHz
PVCC5
VCC
USBVCC
GND_USB
PC_BEEP
KBDCS#
RSTDRV#
IOW#
IOR#
IRQ12
IRQ1
SYSCLK
A20GATE
RCIN#
SD[0..7]
USB_PLUS0
USB_MINUS0
USB0_DAT+
USB0_DAT-
USB_PLUS1
USB_MINUS1
USB_OCH0
MSCLK
MSDATA
KBDATA
KBCLK
KSTB0
KSTB1
KSTB2
KSTB3
KSTB4
KSTB5
KRTN0
KRTN1
KRTN2
KRTN3
KRTN4
SA2
RES#
CS#
XIN
XOUT
CNVSS
VSS
VCC
R222 47K
R223 47K
R224 47K
R225 10K
R226 (0)
R227 0
R228 33
R230 (0)
R231 0
R232 10K
R233 0
R234 0
R235 15K
R236 15K
R342 1K
R343 10K
R229
C328 47PFx6
C342 47PFx4
C343 47PFX5
C345
C329
C330
C331
C332
C333
C334 0.1UF
C335
C336
C337
C338
C339
C340 330PF
C341 18PF
C344
C346 18PF
C347 0.01UF
C348 10UF(3216)
C349 0.1UF
C350 56UF/10V(rubycon-ZAV)
C351 100UF/16V
C352 47PF
C353 47PF
C354 1000PF
C355 0.1UF
C356 0.1UF
C357 0.1UF
C358 0.1UF
C359 470PF
C453 330PF
C495 ?
FB49 BF20S60R2F
FB50 BLM21
FB51 BLM21
FB52 BLM21
FB53 BLM2
FB54 BLM21P300S
FB55 BLM21P300S
FB81 CIM31
FB82 CIM31
FB83 CIM31
FB84 CIM31
CN12 FRAME
CN13 FRAME
CN20 FRAME
CN28 FRAME
CN29 FRAME
IC16 : 7PIN -- GND
14PIN -- VCC5
IC29 : 7PIN -- GND
14PIN -- VCC5


1-15 POWER FAN Controll
CN26
53014-0310
CN27
53014-0310
MLOCK
VFAN
26
R335
5.6
C438
0.1UF
C437
10UF/16V
IC48
KIA78DL09F
GND
OUT
IN
C436
0.1UF
Q14
2SJ187
R237
10K
+12V
Q15
DTC114YK
FANON
26,33
ACL#
26
PVCC5
F2
3.15A/250V
C499
0.1UF
VCC5
-12V
+12V
CN28
5483-15AX
PHSNS
PHOLD
26
14,26,27
C362
270UF/10V OS
C363
0.1UF
C366
0.1UF
C361
47UF/25V
C365
47UF/25V
C360
47UF/25V
C364
47UF/25V

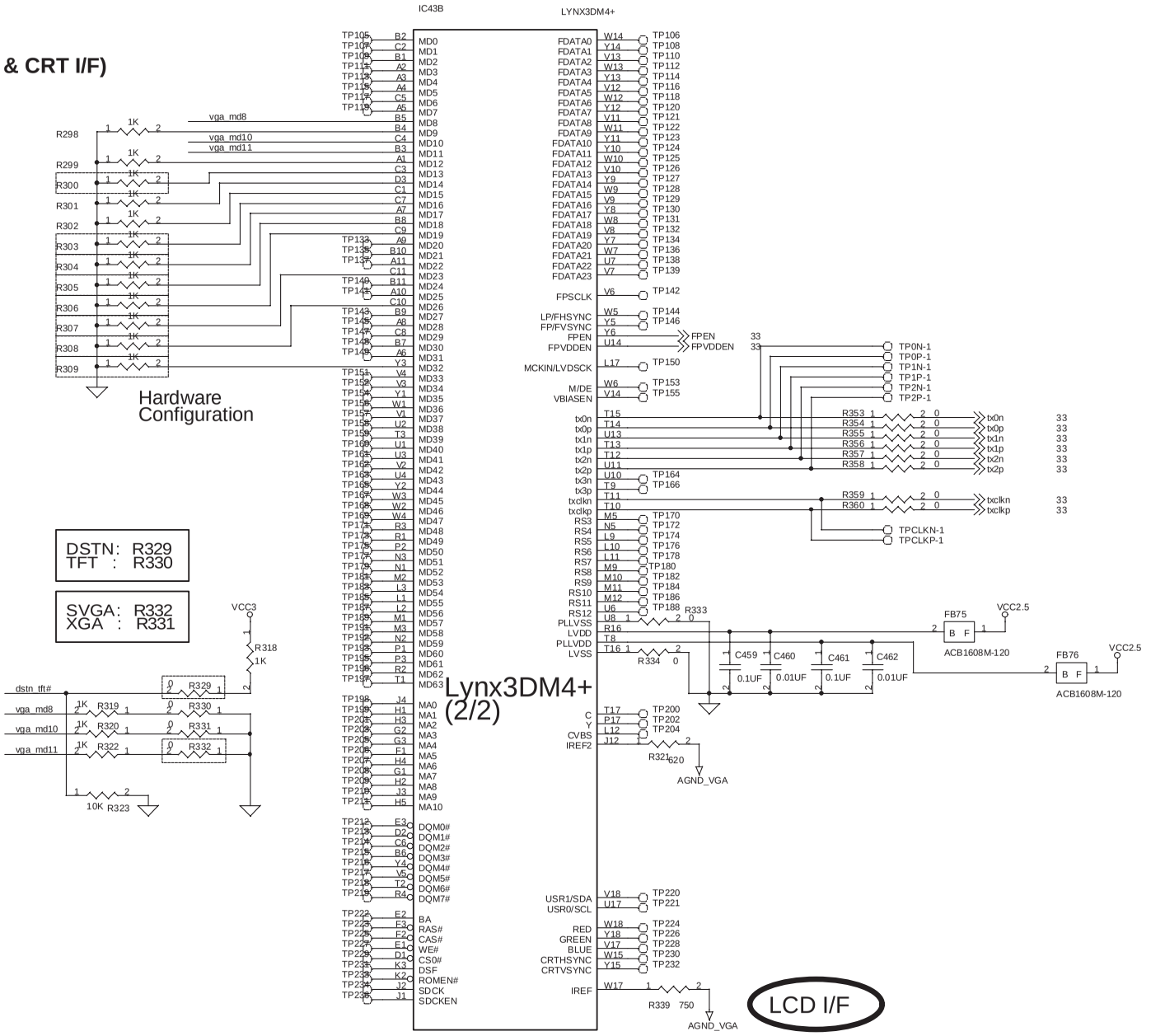

1-16 LAN
RTL8139CL
IC45
IC46
M93C46-W
TLA-6T207
The shield of the connector
LAN ANALOG POWER PLANE
LAN ANALOG GND PLANE
LAN_CLK_PCI_LAN
LAN_RST_PCI_LAN
LAN_REQ#_LAN
LAN_GNT#_LAN
LAN_INTA#_LAN
LAN_IDSEL_LAN
LAN_PCIRST#
LAN_AD[0..31]
LAN_CBE[0..3]#
LAN_FRAME#
LAN_IRDY#
LAN_TRDY#
LAN_DEVSEL#
LAN_STOP#
LAN_PERR#
LAN_SERR#
LAN_PAR
LAN_PME_LAN#

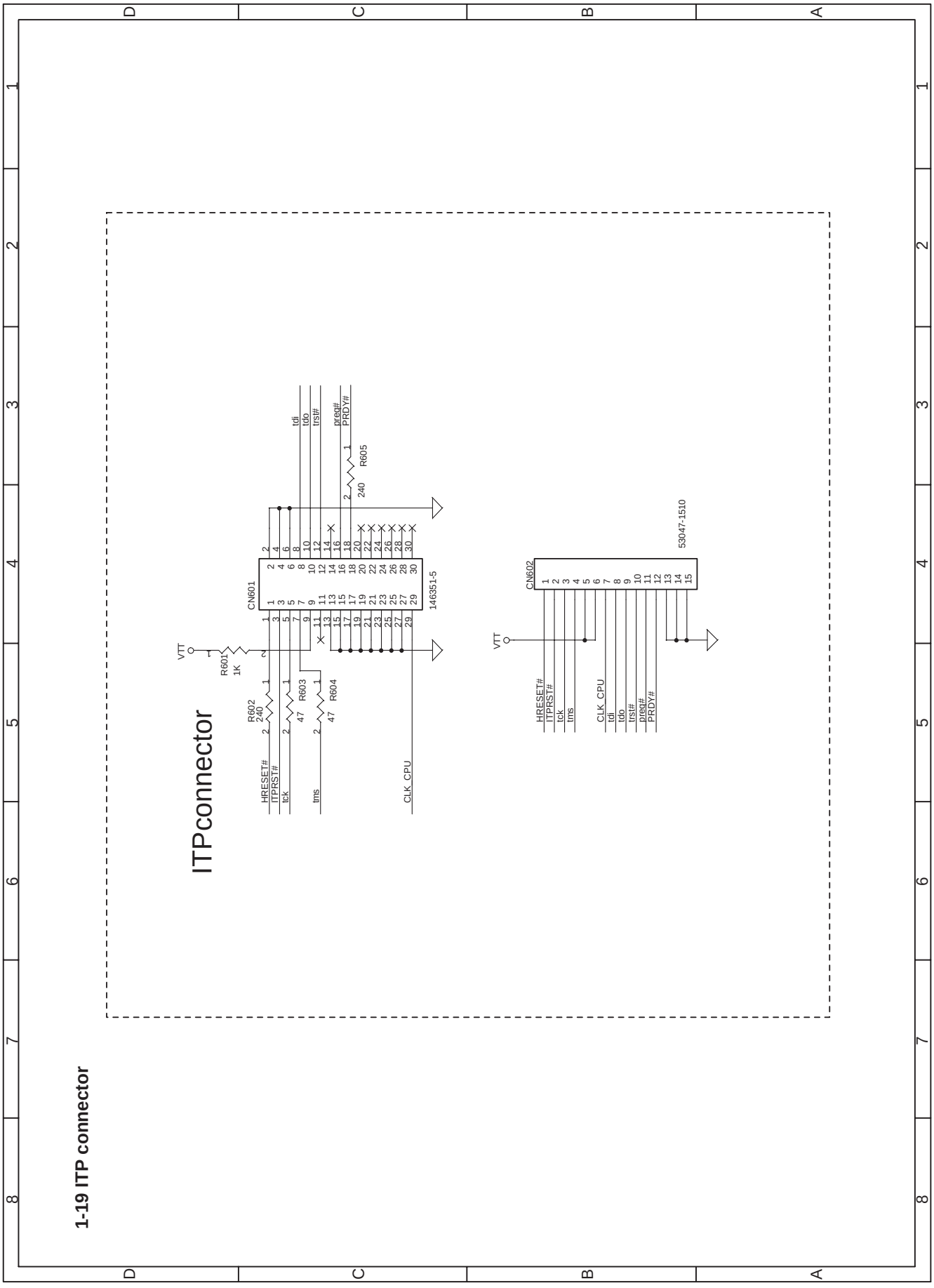

1-17 SLOT
CN30
20-5061-100-052-XXX
-12V
+12V
PVCC5
VCC3
INTD#
CLK_PCI_RISER0
REQ#_RISER0
C/BE#3
C/BE#2
C/BE#1
C/BE#0
IRDY#
DEVSEL#
PLOCK#
PERR#
SERR#
FRAME#
TRDY#
STOP#
SDONE
SBO#
CPAR
PCIRST#
INTA#
GNT#_RISER0
AD[0..31]


1-18-1 VGA (AGP I/F)
CLOCK
AGP interface
Lynx3DM4+ (1/2)
CLOCK
VGA AGP&POWER
3DM/+
EM


1-18-2 VGA
VR1 20K VR
VR2 200K VR
R296 20KF
VR2-2
VR2-1
R370 0
VR1 FRAME GROUND
CN34
53047-1410
VCC
FB86
FB87
FB88
FB89
C463 ?
C464 ?
TPRST#
RXD
TXD
BKLT
VR2-1
VR2-2
F4
ICP0.5
R344 0
+12V
26
26
CN31
53047-1510
txout0n
txout0p
txout1n
txout1p
txout2n
txout2p
txoutclkn
txoutclkp
-12V
R294 10K
C490 1UF/50V
VCC3
D3.3V
VCC5
FPVDD
Q17
Si9948DY
S1 G1 S2 G2
D1 D1 D2 D2
VDC1
VEEP
IC44C
74HCT08
TPRST#
RSTDRV#
15,17,27
C477 ?
C444 220UF/6.3V OS
C430 0.1UF
C429 1UF
FB72
FB73
FB74
BLM21*3
VEEP
IC44A
74HCT08
BKLT
FPEN
BLON
26
34
IC44B
74HCT08
FPVDD
FPVDDEN
34
IC44D
74HCT08
TP0N-2
TP0P-2
TP1N-2
TP1P-2
TP2N-2
TP2P-2
TPCLKN-2
TPCLKP-2
R345 R346 R347 R348 R349 R350 R351 R352
R310 R311 R312 R313 R314 R315 R316 R317
22
txi0n
txi0p
txi1n
txi1p
txi2n
txi2p
txiclkn
txiclkp
C445 20PF
C446 20PF
C447 20PF
C448 20PF
C449 20PF
C450 15PF
C451 15PF
C452 20PF

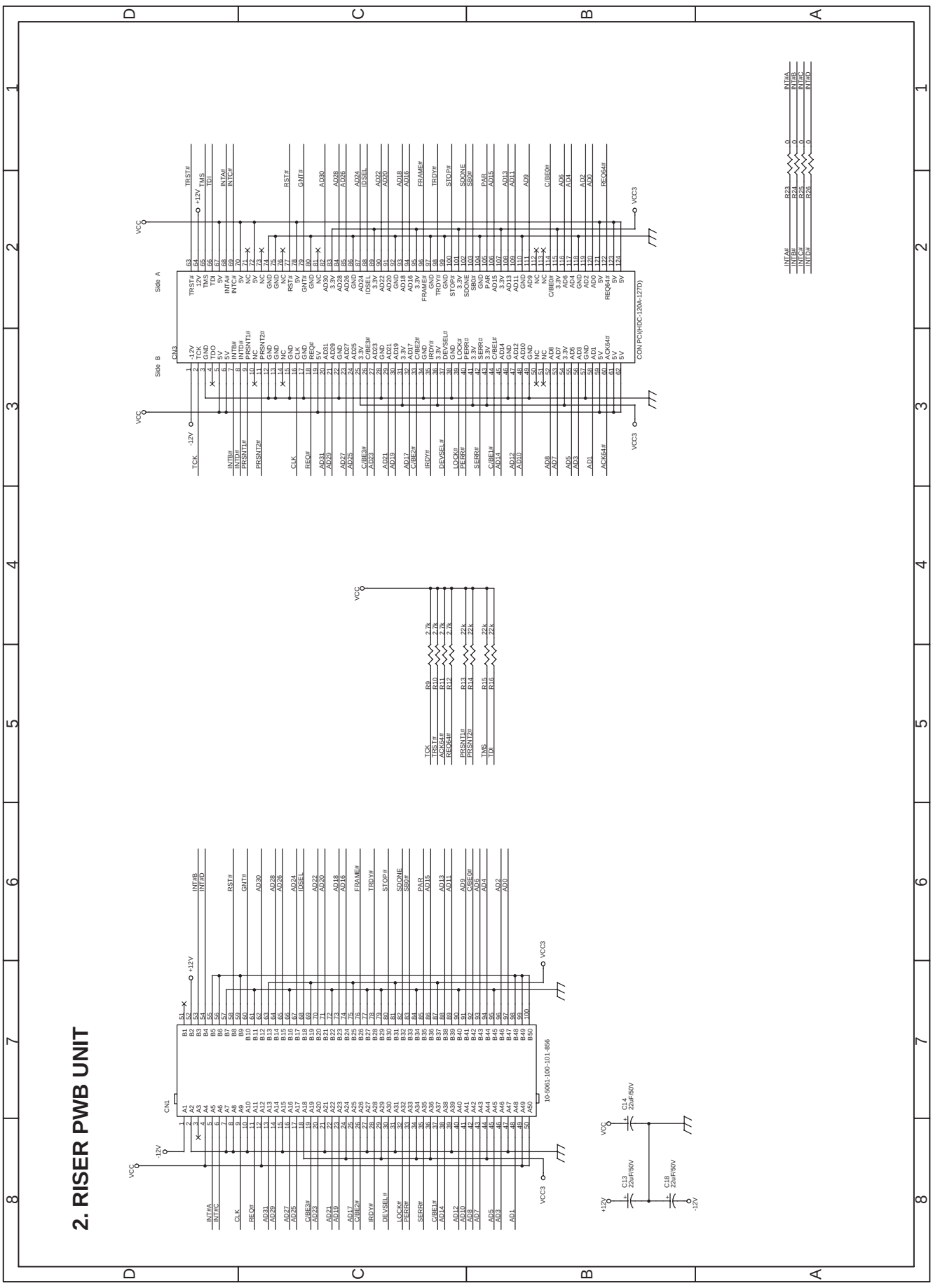
1-18-3 VGA (LCD & CRT I/F)

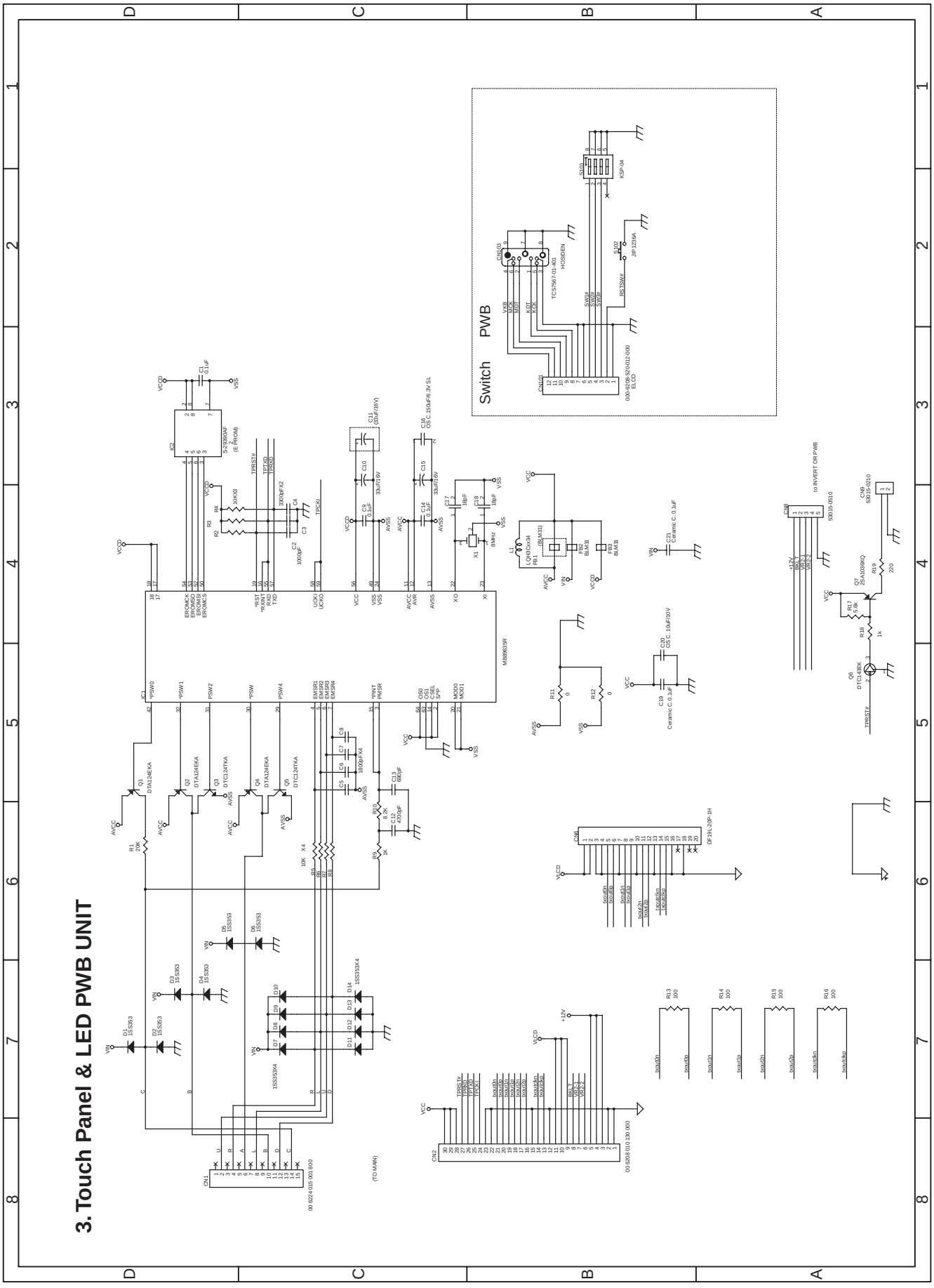


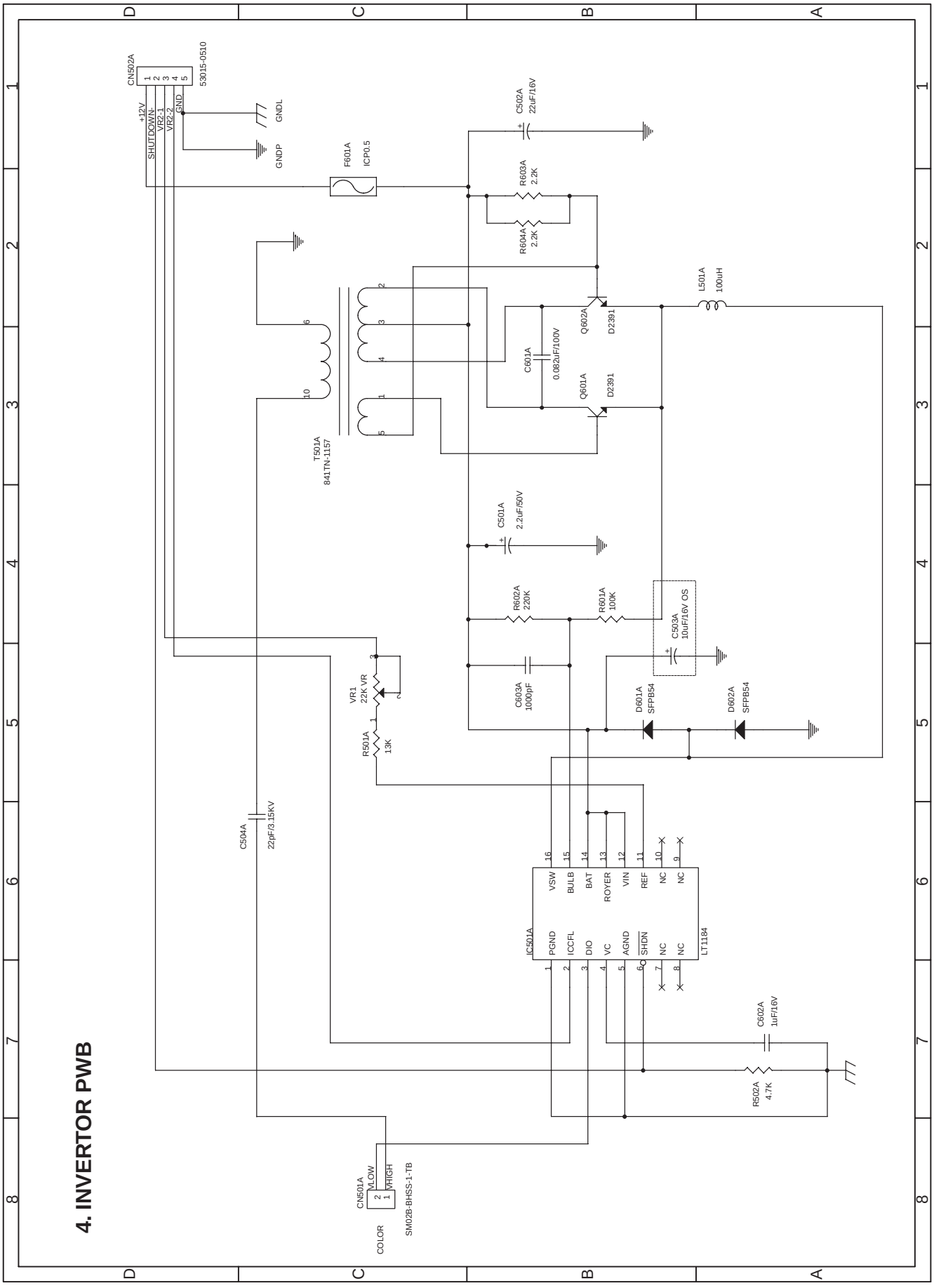


1-19 ITP connector

2. RISER PWB UNIT



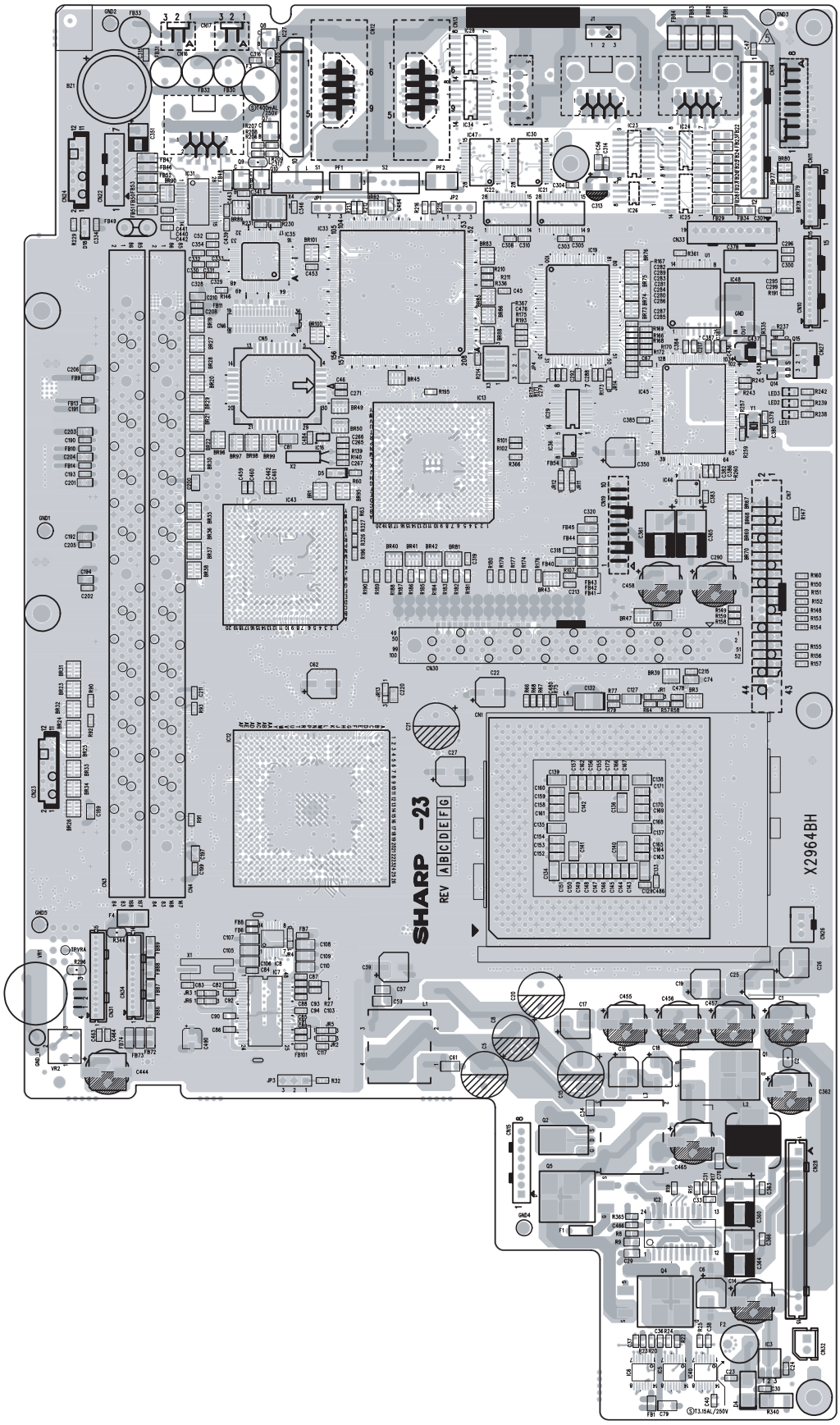

3. Touch Panel & LED PWB UNIT
Switch PWB
MB89635R
(TO MAIN)
to INVERT OR PWB

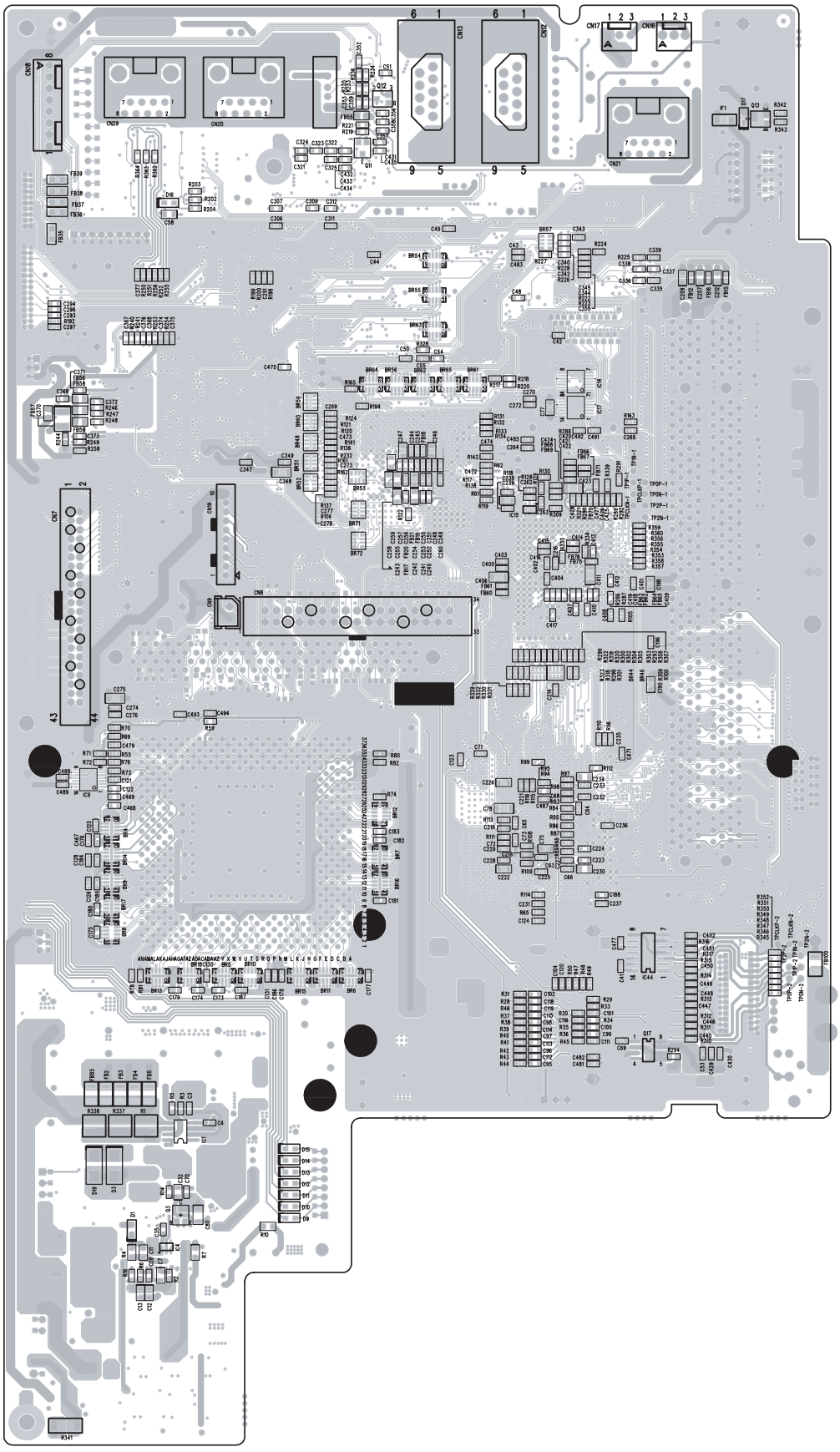

4. INVERTOR PWB
CN502A
53015-0510
+12V
SHUTDOWN-
VR2-1
VR2-2
GND
GNDL
GNDP
F601A
ICP0.5
C502A
22uF/16V
R603A
2.2K
R604A
2.2K
L501A
100uH
Q602A
D2391
C601A
0.082uF/100V
Q601A
D2391
T501A
841TN-1157
C501A
2.2uF/50V
R602A
220K
R601A
100K
C503A
10uF/16V OS
C603A
1000pF
D601A
SFPB54
D602A
SFPB54
VR1
22K VR
R501A
13K
C504A
22pF/3.15KV
IC501A
LT1184
VSW
BULB
BAT
ROYER
VIN
REF
NC
NC
PGND
ICCFL
DIO
VC
AGND
SHDN
NC
NC
C602A
1uF/16V
R502A
4.7K
CN501A
LOW
HIGH
COLOR
SM02B-BHSS-1-TB

CHAPTER 10. PWB LAYOUT

MAIN PWB

UPPER SIDE

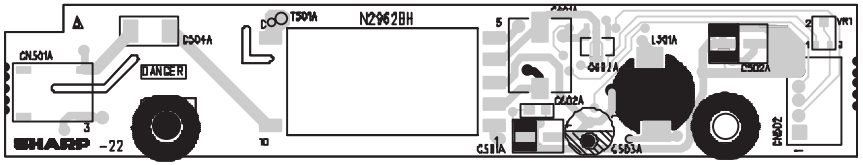




BOTTOM SIDE

INVERTER PWB

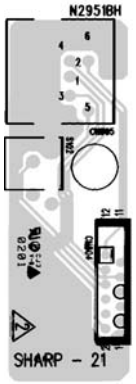
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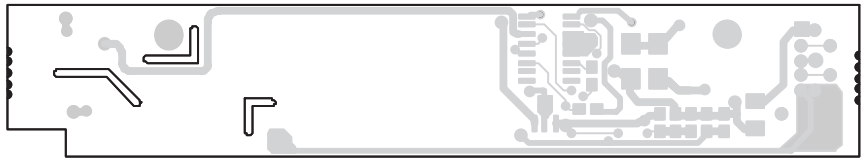
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UPPER SIDE



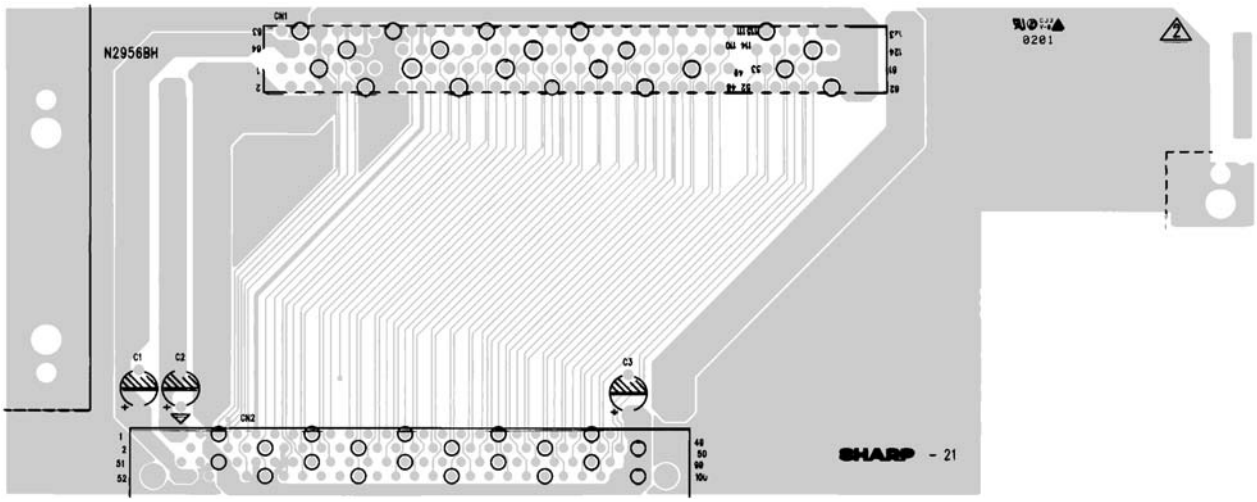
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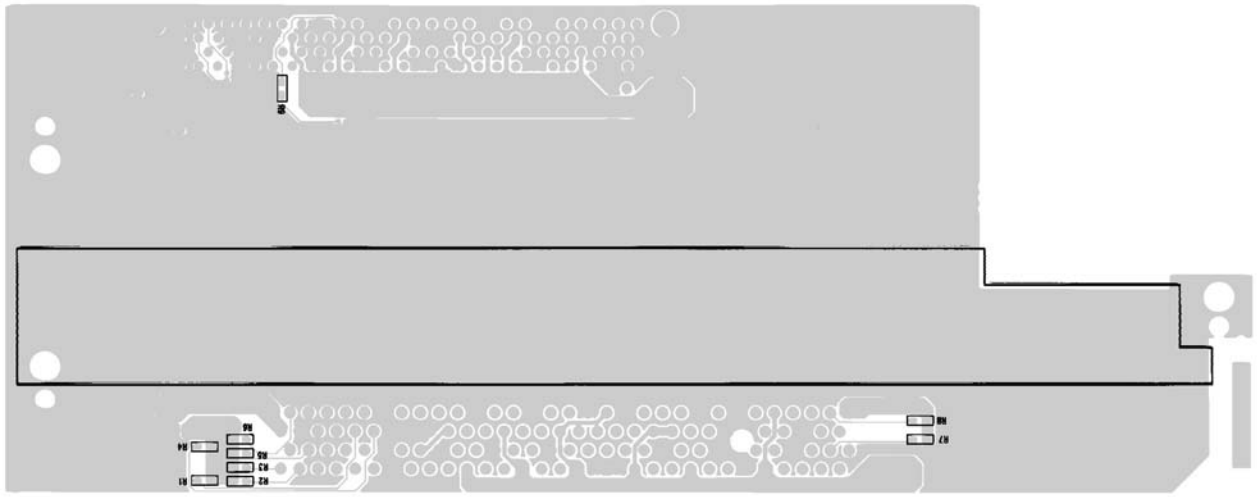
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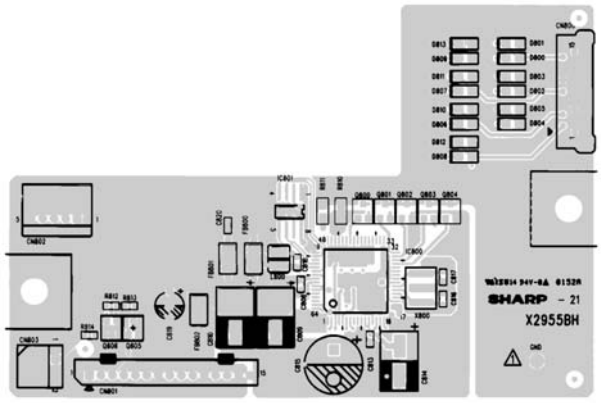
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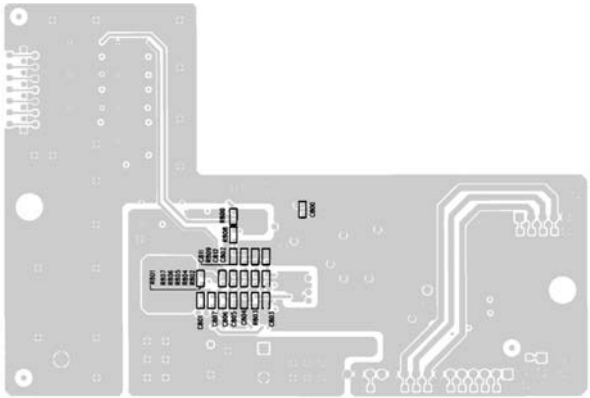
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UPPER SIDE



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